Arquitectura de rango medio mejorada de Microchip (PIC16F1938)

- 49 instrucciones → añaden instrucciones para mejor manejo del uC y para optimización de “C”
- Guardado automático del contexto en las interrupciones → guarda registros principales
- Pila hardware de 16 niveles con overflow y underflow y acceso al contenido
- Acceso lineal a la memoria de programa /datos como memoria única mediante FSR/INDF
- Extremo bajo consumo
- Oscilador mejorado, con cristal, oscilador interno, etc. + PLL para subir frecuencia (hasta 32Mhz)
- Periféricos nuevos o mejorados
  - Registros LAT → evitan problemas en acceso a los puertos
  - DAC de 32 niveles
  - EUSART → hasta 115kbps full-duplax con detección automática de velocidad
  - FVR(Fixed Voltage Feference)
  - Módulo de control de LCD → permite controlar directamente un panel LCD (sin controlador)
  - SR latch
  - Hasta 2 CCP + 3 ECCP (con más modos PWM)
  - Hasta 5 timers ->TMR0, TMR1 y TMR2/4/6 iguales a TMR2 “normal”
  - Módulo sensor capacitivo → monitoriza entradas con cambio de capacidad

Organización de la memoria

- 32 bancos de memoria RAM !!!!! → en cada banco:
  - Los 12 registros principales (se repiten en todos los bancos)
  - Hasta 20 SFR (muchos se repiten)
  - Hasta 80 registros de propósito general (GPR)
  - 16 bytes de RAM comunes a todos los bancos
- Hasta 32K de memoria de programa
- Posibilidad de acceso lineal a la memoria
  - Direccionamiento “normal” → por una lado está la memoria de datos (en bancos) y por otro la de programa
  - Direccionamiento lineal
    - Se ve todo (datos y programa) como un espacio lineal
      - Todos los bancos seguidos a partir de 0x2000
      - La memoria de programa a partir de 0x8000 (sólo se puede acceder a los 8 bits menos significativos de cada posición)
    - Se accede mediante FSRx/INDFx → fig 3-12 y 3-13
      - Registros FSR0 y FSR1 (cada uno 16 bits) → punteros
      - Registros virtuales INDF0 e INDF1 → al usarlos en el código se accede a las posiciones apuntadas por FSR0 y FSR1

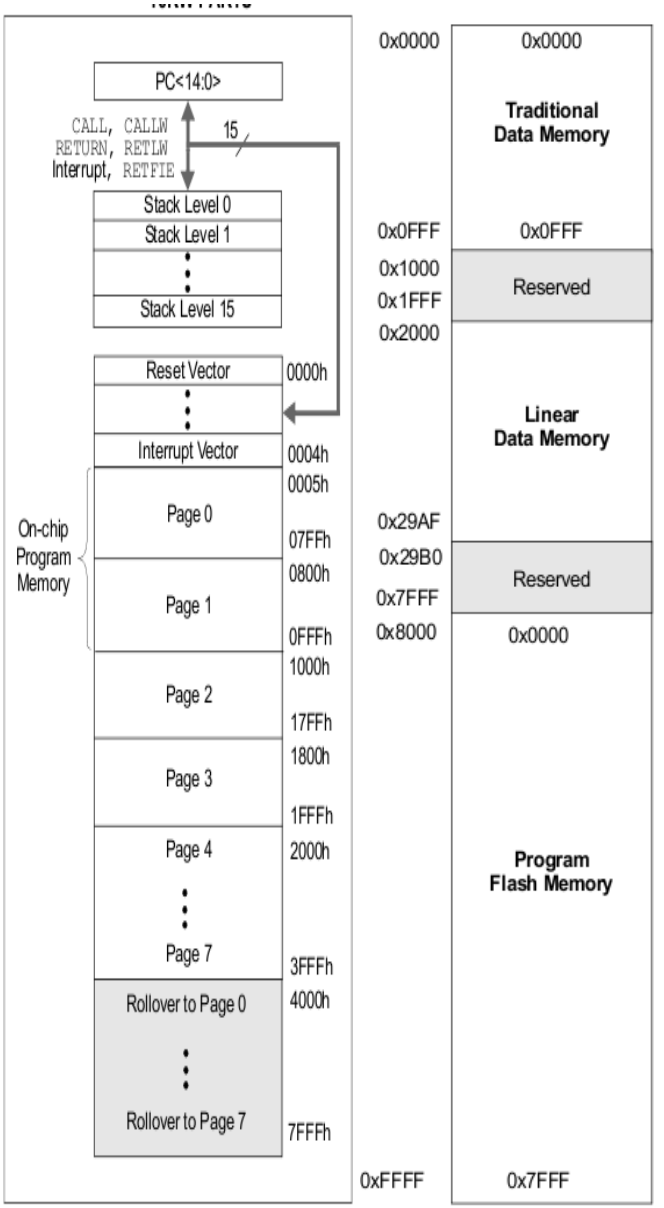


FIGURE 3-11: TRADITIONAL DATA MEMORY MAP

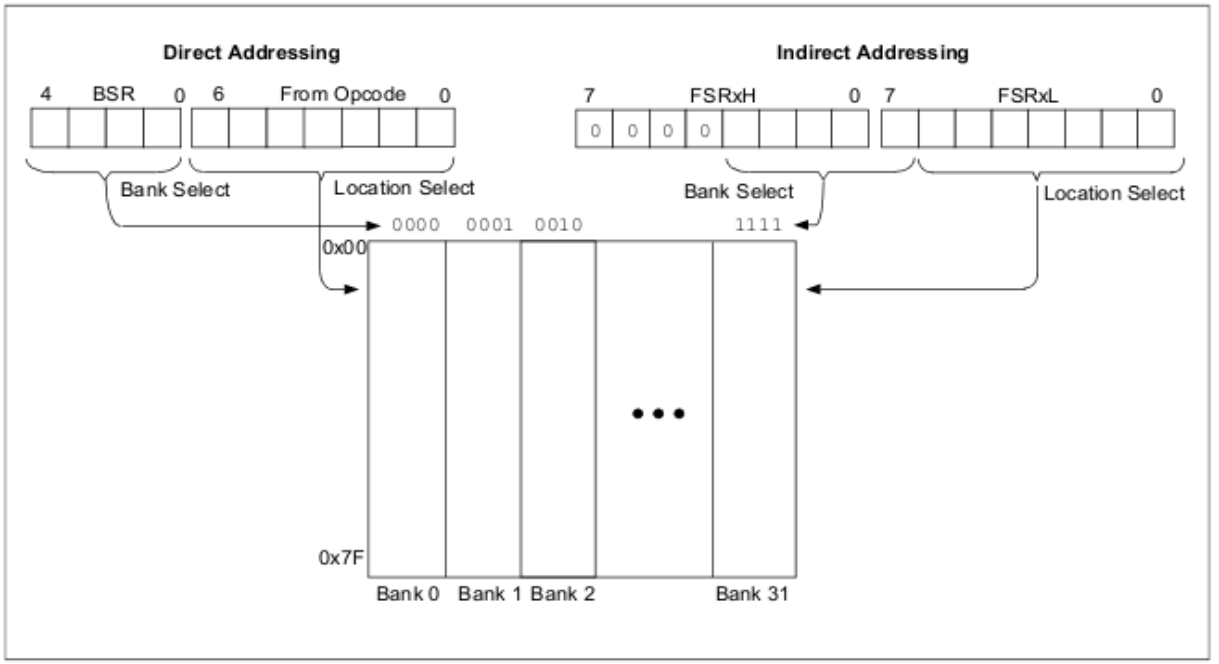


FIGURE 3-12: LINEAR DATA MEMORY MAP

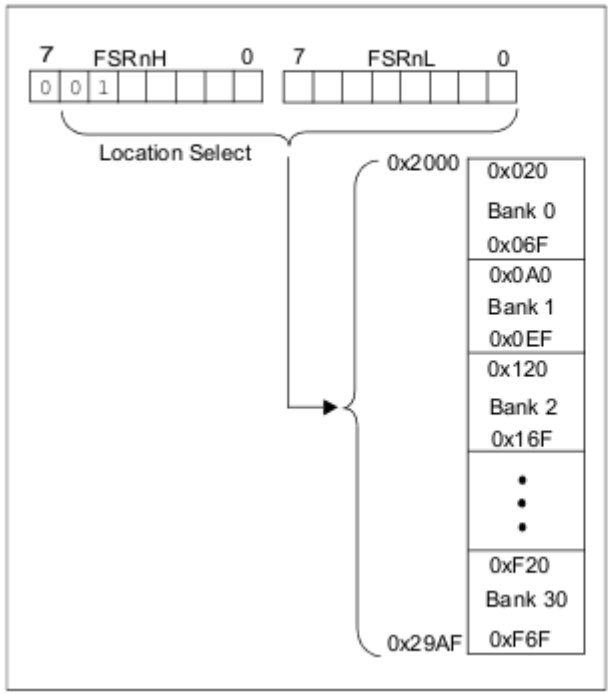


FIGURE 3-13: PROGRAM FLASH MEMORY MAP

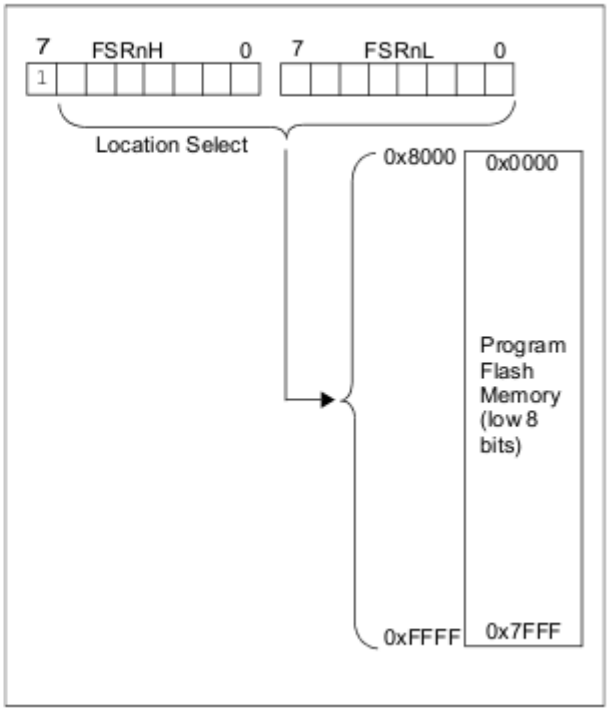


TABLE 3-7: PIC16F1938/1939 MEMORY MAP, BANKS 0-7

	BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7
000h	INDF0	080h	INDF0	100h	INDF0	180h	INDF0	200h	INDF0	280h	INDF0	300h	INDF0	380h	INDF0
001h	INDF1	081h	INDF1	101h	INDF1	181h	INDF1	201h	INDF1	281h	INDF1	301h	INDF1	381h	INDF1
002h	PCL	082h	PCL	102h	PCL	182h	PCL	202h	PCL	282h	PCL	302h	PCL	382h	PCL
003h	STATUS	083h	STATUS	103h	STATUS	183h	STATUS	203h	STATUS	283h	STATUS	303h	STATUS	383h	STATUS
004h	FSR0L	084h	FSR0L	104h	FSR0L	184h	FSR0L	204h	FSR0L	284h	FSR0L	304h	FSR0L	384h	FSR0L
005h	FSR0H	085h	FSR0H	105h	FSR0H	185h	FSR0H	205h	FSR0H	285h	FSR0H	305h	FSR0H	385h	FSR0H
006h	FSR1L	086h	FSR1L	106h	FSR1L	186h	FSR1L	206h	FSR1L	286h	FSR1L	306h	FSR1L	386h	FSR1L
007h	FSR1H	087h	FSR1H	107h	FSR1H	187h	FSR1H	207h	FSR1H	287h	FSR1H	307h	FSR1H	387h	FSR1H
008h	BSR	088h	BSR	108h	BSR	188h	BSR	208h	BSR	288h	BSR	308h	BSR	388h	BSR
009h	WREG	089h	WREG	109h	WREG	189h	WREG	209h	WREG	289h	WREG	309h	WREG	389h	WREG
00Ah	PCLATH	08Ah	PCLATH	10Ah	PCLATH	18Ah	PCLATH	20Ah	PCLATH	28Ah	PCLATH	30Ah	PCLATH	38Ah	PCLATH
00Bh	INTCON	08Bh	INTCON	10Bh	INTCON	18Bh	INTCON	20Bh	INTCON	28Bh	INTCON	30Bh	INTCON	38Bh	INTCON
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	—	28Ch	—	30Ch	—	38Ch	—
00Dh	PORTB	08Dh	TRISB	10Dh	LATB	18Dh	ANSELB	20Dh	WPUB	28Dh	—	30Dh	—	38Dh	—
00Eh	PORTC	08Eh	TRISC	10Eh	LATC	18Eh	—	20Eh	—	28Eh	—	30Eh	—	38Eh	—
00Fh	PORTD(1)	08Fh	TRISD(1)	10Fh	LATD(1)	18Fh	ANSELD(1)	20Fh	—	28Fh	—	30Fh	—	38Fh	—
010h	PORTE	090h	TRISE	110h	LATE(1)	190h	ANSELE(1)	210h	WPUE	290h	—	310h	—	390h	—
011h	PIR1	091h	PIE1	111h	CM1CON0	191h	EEADRL	211h	SSPxBUF	291h	CCPR1L	311h	CCPR3L	391h	—
012h	PIR2	092h	PIE2	112h	CM1CON1	192h	EEADRH	212h	SSPxADD	292h	CCPR1H	312h	CCPR3H	392h	—
013h	PIR3	093h	PIE3	113h	CM2CON0	193h	EEDATL	213h	SSPxMSK	293h	CCP1CON	313h	CCP3CON	393h	—
014h	—	094h	—	114h	CM2CON1	194h	EEDATH	214h	SSPxSTAT	294h	PWM1CON	314h	PWM3CON	394h	IOCBP
015h	TMR0	095h	OPTION	115h	CMOUT	195h	EECON1	215h	SSPxCON1	295h	CCP1AS	315h	CCP3AS	395h	IOCBN
016h	TMR1L	096h	PCON	116h	BORCON	196h	EECON2	216h	SSPxCON2	296h	PSTR1CON	316h	PSTR3CON	396h	IOCBF
017h	TMR1H	097h	WDTCON	117h	FVRCON	197h	—	217h	SSPxCON3	297h	—	317h	—	397h	—
018h	T1CON	098h	OSCTUNE	118h	DACCON0	198h	—	218h	—	298h	CCPR2L	318h	CCPR4L	398h	—
019h	T1GCON	099h	OSCCON	119h	DACCON1	199h	RC1REG	219h	—	299h	CCPR2H	319h	CCPR4H	399h	—
01Ah	TMR2	09Ah	OSCSTAT	11Ah	SRCON0	19Ah	TX1REG	21Ah	—	29Ah	CCP2CON	31Ah	CCP4CON	39Ah	—
01Bh	PR2	09Bh	ADRESL	11Bh	SRCON1	19Bh	SPBRGL	21Bh	—	29Bh	PWM2CON	31Bh	—	39Bh	—
01Ch	T2CON	09Ch	ADRESH	11Ch	—	19Ch	SPBRGH	21Ch	—	29Ch	CCP2AS	31Ch	CCPR5L	39Ch	—
01Dh	—	09Dh	ADCON0	11Dh	APFCON	19Dh	RCSTA	21Dh	—	29Dh	PSTR2CON	31Dh	CCPR5H	39Dh	—
01Eh	CPSCON0	09Eh	ADCON1	11Eh	—	19Eh	TXSTA	21Eh	—	29Eh	CCPTMRS0	31Eh	CCP5CON	39Eh	—
01Fh	CPSCON1	09Fh	—	11Fh	—	19Fh	BAUDCON	21Fh	—	29Fh	CCPTMRS1	31Fh	—	39Fh	—
020h 06Fh	General Purpose Register 96 Bytes	0A0h 0EFh	General Purpose Register 80 Bytes	120h 16Fh	General Purpose Register 80 Bytes	1A0h 1EFh	General Purpose Register 80 Bytes	220h 26Fh	General Purpose Register 80 Bytes	2A0h 2EFh	General Purpose Register 80 Bytes	320h 32Fh 330h 36Fh	General Purpose Register 80 Bytes	3A0h 3EFh	General Purpose Register 80 Bytes
070h 07Fh	Accesses 70h – 7Fh	0F0h 0FFh	Accesses 70h – 7Fh	170h 17Fh	Accesses 70h – 7Fh	1F0h 1FFh	Accesses 70h – 7Fh	270h 27Fh	Accesses 70h – 7Fh	2F0h 2FFh	Accesses 70h – 7Fh	370h 37Fh	Accesses 70h – 7Fh	3F0h 3FFh	Accesses 70h – 7Fh

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: Not available on PIC16F1933/1936/1938/PIC16LF1933/1936/1938.

TABLE 3-8: PIC16F1938/1939 MEMORY MAP, BANKS 8-15

	BANK 8		BANK 9		BANK 10		BANK 11		BANK 12		BANK 13		BANK 14		BANK 15
400h	INDF0	480h	INDF0	500h	INDF0	580h	INDF0	600h	INDF0	680h	INDF0	700h	INDF0	780h	INDF0
401h	INDF1	481h	INDF1	501h	INDF1	581h	INDF1	601h	INDF1	681h	INDF1	701h	INDF1	781h	INDF1
402h	PCL	482h	PCL	502h	PCL	582h	PCL	602h	PCL	682h	PCL	702h	PCL	782h	PCL
403h	STATUS	483h	STATUS	503h	STATUS	583h	STATUS	603h	STATUS	683h	STATUS	703h	STATUS	783h	STATUS
404h	FSR0L	484h	FSR0L	504h	FSR0L	584h	FSR0L	604h	FSR0L	684h	FSR0L	704h	FSR0L	784h	FSR0L
405h	FSR0H	485h	FSR0H	505h	FSR0H	585h	FSR0H	605h	FSR0H	685h	FSR0H	705h	FSR0H	785h	FSR0H
406h	FSR1L	486h	FSR1L	506h	FSR1L	586h	FSR1L	606h	FSR1L	686h	FSR1L	706h	FSR1L	786h	FSR1L
407h	FSR1H	487h	FSR1H	507h	FSR1H	587h	FSR1H	607h	FSR1H	687h	FSR1H	707h	FSR1H	787h	FSR1H
408h	BSR	488h	BSR	508h	BSR	588h	BSR	608h	BSR	688h	BSR	708h	BSR	788h	BSR
409h	WREG	489h	WREG	509h	WREG	589h	WREG	609h	WREG	689h	WREG	709h	WREG	789h	WREG
40Ah	PCLATH	48Ah	PCLATH	50Ah	PCLATH	58Ah	PCLATH	60Ah	PCLATH	68Ah	PCLATH	70Ah	PCLATH	78Ah	PCLATH
40Bh	INTCON	48Bh	INTCON	50Bh	INTCON	58Bh	INTCON	60Bh	INTCON	68Bh	INTCON	70Bh	INTCON	78Bh	INTCON
40Ch	—	48Ch	—	50Ch	—	58Ch	—	60Ch	—	68Ch	—	70Ch	—	78Ch	—
40Dh	—	48Dh	—	50Dh	—	58Dh	—	60Dh	—	68Dh	—	70Dh	—	78Dh	—
40Eh	—	48Eh	—	50Eh	—	58Eh	—	60Eh	—	68Eh	—	70Eh	—	78Eh	—
40Fh	—	48Fh	—	50Fh	—	58Fh	—	60Fh	—	68Fh	—	70Fh	—	78Fh	—
410h	—	490h	—	510h	—	590h	—	610h	—	690h	—	710h	—	790h	—
411h	—	491h	—	511h	—	591h	—	611h	—	691h	—	711h	—	791h	See Table 3-11 or Table 3-12
412h	—	492h	—	512h	—	592h	—	612h	—	692h	—	712h	—	792h	
413h	—	493h	—	513h	—	593h	—	613h	—	693h	—	713h	—	793h	
414h	—	494h	—	514h	—	594h	—	614h	—	694h	—	714h	—	794h	
415h	TMR4	495h	—	515h	—	595h	—	615h	—	695h	—	715h	—	795h	
416h	PR4	496h	—	516h	—	596h	—	616h	—	696h	—	716h	—	796h	
417h	T4CON	497h	—	517h	—	597h	—	617h	—	697h	—	717h	—	797h	
418h	—	498h	—	518h	—	598h	—	618h	—	698h	—	718h	—	798h	
419h	—	499h	—	519h	—	599h	—	619h	—	699h	—	719h	—	799h	
41Ah	—	49Ah	—	51Ah	—	59Ah	—	61Ah	—	69Ah	—	71Ah	—	79Ah	
41Bh	—	49Bh	—	51Bh	—	59Bh	—	61Bh	—	69Bh	—	71Bh	—	79Bh	
41Ch	TMR6	49Ch	—	51Ch	—	59Ch	—	61Ch	—	69Ch	—	71Ch	—	79Ch	
41Dh	PR6	49Dh	—	51Dh	—	59Dh	—	61Dh	—	69Dh	—	71Dh	—	79Dh	
41Eh	T6CON	49Eh	—	51Eh	—	59Eh	—	61Eh	—	69Eh	—	71Eh	—	79Eh	
41Fh	—	49Fh	—	51Fh	—	59Fh	—	61Fh	—	69Fh	—	71Fh	—	79Fh	
420h	General Purpose Register 80 Bytes	4A0h	General Purpose Register 80 Bytes	520h	General Purpose Register 80 Bytes	5A0h	General Purpose Register 80 Bytes	620h	General Purpose Register 48 Bytes	6A0h	Unimplemented Read as '0'	720h	Unimplemented Read as '0'	7A0h	
46Fh		4EFh		56Fh		5EFh		66Fh	Unimplemented Read as '0'	6EFh		76Fh		7EFh	
470h	Accesses 70h – 7Fh	4F0h	Accesses 70h – 7Fh	570h	Accesses 70h – 7Fh	5F0h	Accesses 70h – 7Fh	670h	Accesses 70h – 7Fh	6F0h	Accesses 70h – 7Fh	770h	Accesses 70h – 7Fh	7F0h	Accesses 70h – 7Fh
47Fh		4FFh		57Fh		5FFh		67Fh		6FFh		77Fh		7FFh	

Legend: = Unimplemented data memory locations, read as '0'.

TABLE 3-9: PIC16F193X/LF193X MEMORY MAP, BANKS 16-23

	BANK 16		BANK 17		BANK 18		BANK 19		BANK 20		BANK 21		BANK 22		BANK 23
800h	INDF0	880h	INDF0	900h	INDF0	980h	INDF0	A00h	INDF0	A80h	INDF0	B00h	INDF0	B80h	INDF0
801h	INDF1	881h	INDF1	901h	INDF1	981h	INDF1	A01h	INDF1	A81h	INDF1	B01h	INDF1	B81h	INDF1
802h	PCL	882h	PCL	902h	PCL	982h	PCL	A02h	PCL	A82h	PCL	B02h	PCL	B82h	PCL
803h	STATUS	883h	STATUS	903h	STATUS	983h	STATUS	A03h	STATUS	A83h	STATUS	B03h	STATUS	B83h	STATUS
804h	FSR0L	884h	FSR0L	904h	FSR0L	984h	FSR0L	A04h	FSR0L	A84h	FSR0L	B04h	FSR0L	B84h	FSR0L
805h	FSR0H	885h	FSR0H	905h	FSR0H	985h	FSR0H	A05h	FSR0H	A85h	FSR0H	B05h	FSR0H	B85h	FSR0H
806h	FSR1L	886h	FSR1L	906h	FSR1L	986h	FSR1L	A06h	FSR1L	A86h	FSR1L	B06h	FSR1L	B86h	FSR1L
807h	FSR1H	887h	FSR1H	907h	FSR1H	987h	FSR1H	A07h	FSR1H	A87h	FSR1H	B07h	FSR1H	B87h	FSR1H
808h	BSR	888h	BSR	908h	BSR	988h	BSR	A08h	BSR	A88h	BSR	B08h	BSR	B88h	BSR
809h	WREG	889h	WREG	909h	WREG	989h	WREG	A09h	WREG	A89h	WREG	B09h	WREG	B89h	WREG
80Ah	PCLATH	88Ah	PCLATH	90Ah	PCLATH	98Ah	PCLATH	A0Ah	PCLATH	A8Ah	PCLATH	B0Ah	PCLATH	B8Ah	PCLATH
80Bh	INTCON	88Bh	INTCON	90Bh	INTCON	98Bh	INTCON	A0Bh	INTCON	A8Bh	INTCON	B0Bh	INTCON	B8Bh	INTCON
80Ch	—	88Ch	—	90Ch	—	98Ch	—	A0Ch	—	A8Ch	—	B0Ch	—	B8Ch	—
80Dh	—	88Dh	—	90Dh	—	98Dh	—	A0Dh	—	A8Dh	—	B0Dh	—	B8Dh	—
80Eh	—	88Eh	—	90Eh	—	98Eh	—	A0Eh	—	A8Eh	—	B0Eh	—	B8Eh	—
80Fh	—	88Fh	—	90Fh	—	98Fh	—	A0Fh	—	A8Fh	—	B0Fh	—	B8Fh	—
810h	—	890h	—	910h	—	990h	—	A10h	—	A90h	—	B10h	—	B90h	—
811h	—	891h	—	911h	—	991h	—	A11h	—	A91h	—	B11h	—	B91h	—
812h	—	892h	—	912h	—	992h	—	A12h	—	A92h	—	B12h	—	B92h	—
813h	—	893h	—	913h	—	993h	—	A13h	—	A93h	—	B13h	—	B93h	—
814h	—	894h	—	914h	—	994h	—	A14h	—	A94h	—	B14h	—	B94h	—
815h	—	895h	—	915h	—	995h	—	A15h	—	A95h	—	B15h	—	B95h	—
816h	—	896h	—	916h	—	996h	—	A16h	—	A96h	—	B16h	—	B96h	—
817h	—	897h	—	917h	—	997h	—	A17h	—	A97h	—	B17h	—	B97h	—
818h	—	898h	—	918h	—	998h	—	A18h	—	A98h	—	B18h	—	B98h	—
819h	—	899h	—	919h	—	999h	—	A19h	—	A99h	—	B19h	—	B99h	—
81Ah	—	89Ah	—	91Ah	—	99Ah	—	A1Ah	—	A9Ah	—	B1Ah	—	B9Ah	—
81Bh	—	89Bh	—	91Bh	—	99Bh	—	A1Bh	—	A9Bh	—	B1Bh	—	B9Bh	—
81Ch	—	89Ch	—	91Ch	—	99Ch	—	A1Ch	—	A9Ch	—	B1Ch	—	B9Ch	—
81Dh	—	89Dh	—	91Dh	—	99Dh	—	A1Dh	—	A9Dh	—	B1Dh	—	B9Dh	—
81Eh	—	89Eh	—	91Eh	—	99Eh	—	A1Eh	—	A9Eh	—	B1Eh	—	B9Eh	—
81Fh	—	89Fh	—	91Fh	—	99Fh	—	A1Fh	—	A9Fh	—	B1Fh	—	B9Fh	—
820h 86Fh	Unimplemented Read as '0'	8A0h 8EFh	Unimplemented Read as '0'	920h 96Fh	Unimplemented Read as '0'	9A0h 9EFh	Unimplemented Read as '0'	A20h A6Fh	Unimplemented Read as '0'	AA0h AEFh	Unimplemented Read as '0'	B20h B6Fh	Unimplemented Read as '0'	BA0h BEFh	Unimplemented Read as '0'
870h 87Fh	Accesses 70h – 7Fh	8F0h 8FFh	Accesses 70h – 7Fh	970h 97Fh	Accesses 70h – 7Fh	9F0h 9FFh	Accesses 70h – 7Fh	A70h A7Fh	Accesses 70h – 7Fh	AF0h AFFh	Accesses 70h – 7Fh	B70h B7Fh	Accesses 70h – 7Fh	BF0h BFFh	Accesses 70h – 7Fh

Legend: = Unimplemented data memory locations, read as '0'.

TABLE 3-10: PIC16F193X/LF193X MEMORY MAP, BANKS 24-31

	BANK 24		BANK 25		BANK 26		BANK 27		BANK 28		BANK 29		BANK 30		BANK 31
C00h	INDF0	C80h	INDF0	D00h	INDF0	D80h	INDF0	E00h	INDF0	E80h	INDF0	F00h	INDF0	F80h	INDF0
C01h	INDF1	C81h	INDF1	D01h	INDF1	D81h	INDF1	E01h	INDF1	E81h	INDF1	F01h	INDF1	F81h	INDF1
C02h	PCL	C82h	PCL	D02h	PCL	D82h	PCL	E02h	PCL	E82h	PCL	F02h	PCL	F82h	PCL
C03h	STATUS	C83h	STATUS	D03h	STATUS	D83h	STATUS	E03h	STATUS	E83h	STATUS	F03h	STATUS	F83h	STATUS
C04h	FSR0L	C84h	FSR0L	D04h	FSR0L	D84h	FSR0L	E04h	FSR0L	E84h	FSR0L	F04h	FSR0L	F84h	FSR0L
C05h	FSR0H	C85h	FSR0H	D05h	FSR0H	D85h	FSR0H	E05h	FSR0H	E85h	FSR0H	F05h	FSR0H	F85h	FSR0H
C06h	FSR1L	C86h	FSR1L	D06h	FSR1L	D86h	FSR1L	E06h	FSR1L	E86h	FSR1L	F06h	FSR1L	F86h	FSR1L
C07h	FSR1H	C87h	FSR1H	D07h	FSR1H	D87h	FSR1H	E07h	FSR1H	E87h	FSR1H	F07h	FSR1H	F87h	FSR1H
C08h	BSR	C88h	BSR	D08h	BSR	D88h	BSR	E08h	BSR	E88h	BSR	F08h	BSR	F88h	BSR
C09h	WREG	C89h	WREG	D09h	WREG	D89h	WREG	E09h	WREG	E89h	WREG	F09h	WREG	F89h	WREG
C0Ah	PCLATH	C8Ah	PCLATH	D0Ah	PCLATH	D8Ah	PCLATH	E0Ah	PCLATH	E8Ah	PCLATH	F0Ah	PCLATH	F8Ah	PCLATH
C0Bh	INTCON	C8Bh	INTCON	D0Bh	INTCON	D8Bh	INTCON	E0Bh	INTCON	E8Bh	INTCON	F0Bh	INTCON	F8Bh	INTCON
C0Ch	—	C8Ch	—	D0Ch	—	D8Ch	—	E0Ch	—	E8Ch	—	F0Ch	—	F8Ch	See Table 3-13
C0Dh	—	C8Dh	—	D0Dh	—	D8Dh	—	E0Dh	—	E8Dh	—	F0Dh	—	F8Dh	
C0Eh	—	C8Eh	—	D0Eh	—	D8Eh	—	E0Eh	—	E8Eh	—	F0Eh	—	F8Eh	
C0Fh	—	C8Fh	—	D0Fh	—	D8Fh	—	E0Fh	—	E8Fh	—	F0Fh	—	F8Fh	
C10h	—	C90h	—	D10h	—	D90h	—	E10h	—	E90h	—	F10h	—	F90h	
C11h	—	C91h	—	D11h	—	D91h	—	E11h	—	E91h	—	F11h	—	F91h	
C12h	—	C92h	—	D12h	—	D92h	—	E12h	—	E92h	—	F12h	—	F92h	
C13h	—	C93h	—	D13h	—	D93h	—	E13h	—	E93h	—	F13h	—	F93h	
C14h	—	C94h	—	D14h	—	D94h	—	E14h	—	E94h	—	F14h	—	F94h	
C15h	—	C95h	—	D15h	—	D95h	—	E15h	—	E95h	—	F15h	—	F95h	
C16h	—	C96h	—	D16h	—	D96h	—	E16h	—	E96h	—	F16h	—	F96h	
C17h	—	C97h	—	D17h	—	D97h	—	E17h	—	E97h	—	F17h	—	F97h	
C18h	—	C98h	—	D18h	—	D98h	—	E18h	—	E98h	—	F18h	—	F98h	
C19h	—	C99h	—	D19h	—	D99h	—	E19h	—	E99h	—	F19h	—	F99h	
C1Ah	—	C9Ah	—	D1Ah	—	D9Ah	—	E1Ah	—	E9Ah	—	F1Ah	—	F9Ah	
C1Bh	—	C9Bh	—	D1Bh	—	D9Bh	—	E1Bh	—	E9Bh	—	F1Bh	—	F9Bh	
C1Ch	—	C9Ch	—	D1Ch	—	D9Ch	—	E1Ch	—	E9Ch	—	F1Ch	—	F9Ch	
C1Dh	—	C9Dh	—	D1Dh	—	D9Dh	—	E1Dh	—	E9Dh	—	F1Dh	—	F9Dh	
C1Eh	—	C9Eh	—	D1Eh	—	D9Eh	—	E1Eh	—	E9Eh	—	F1Eh	—	F9Eh	
C1Fh	—	C9Fh	—	D1Fh	—	D9Fh	—	E1Fh	—	E9Fh	—	F1Fh	—	F9Fh	
C20h C6Fh	Unimplemented Read as '0'	CA0h CEFh	Unimplemented Read as '0'	D20h D6Fh	Unimplemented Read as '0'	DA0h DEFh	Unimplemented Read as '0'	E20h E6Fh	Unimplemented Read as '0'	EA0h EEFh	Unimplemented Read as '0'	F20h F6Fh	Unimplemented Read as '0'	FA0h FEFh	
C70h CFFh	Accesses 70h – 7Fh	CF0h CFFh	Accesses 70h – 7Fh	D70h D7Fh	Accesses 70h – 7Fh	DF0h DFFh	Accesses 70h – 7Fh	E70h E7Fh	Accesses 70h – 7Fh	EF0h EFFh	Accesses 70h – 7Fh	F70h F7Fh	Accesses 70h – 7Fh	FF0h FFFh	Accesses 70h – 7Fh

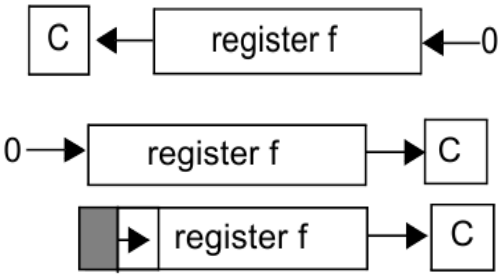
Legend: = Unimplemented data memory locations, read as '0'.

La pila y el salvado automático del contexto de interrución

- Al producirse una interrupción (automáticamente)
  - La dirección de retorno se guarda en la pila
  - Un conjunto de registros se guardan en “Registros sombra” (shadow), en el banco 31
    - Acumulador y STATUS
    - BSR y FSR
    - PCLATH
  - Al volver de la interrupción se recupera la dirección de retorno y los valores de los registros desde los registros sombra
- Pila hardware (no almacenada en memoria de datos) con 16 niveles
  - Direcciones desde 0x00 hasta 0x0F
  - Registro STKPTR → puntero de pila ->Indica la ultima posición usada en la pila (si está vacía 0x1F)
  - Registros TOSH/TOSL → permiten leer/escribir el contenido de la posición apuntada por STKPTR
  - Protección contra overflow/underflow
    - Bit STVREN=1 (palabra de configuración 2) → el overflow/underflow provoca un RESET y no se sobreescribe el valor de la pila
    - Registro PCON, bits STKOVF Y STKUNF → al producirse el overflow/underflow se activan estos bits

Nuevas instrucciones

- BRA ***etiqueta*** → salto relativo (etiqueta entre -255 y +255)
- BRW → salto relativo (posición + acumulador) → evita problemas de páginas en tablas
- MOVLP ***literal*** → PCLATH = literal
- MOVLB ***literal*** → BSR = literal (selección de banco)
- LSLF ***f {,d}*** → desplazamiento lógico a izda.
- LSRF ***f {,d}*** → desplazamiento lógico a dcha.
- ASRF ***f {,d}*** → desp. aritmético a dcha. Mantiene MSB

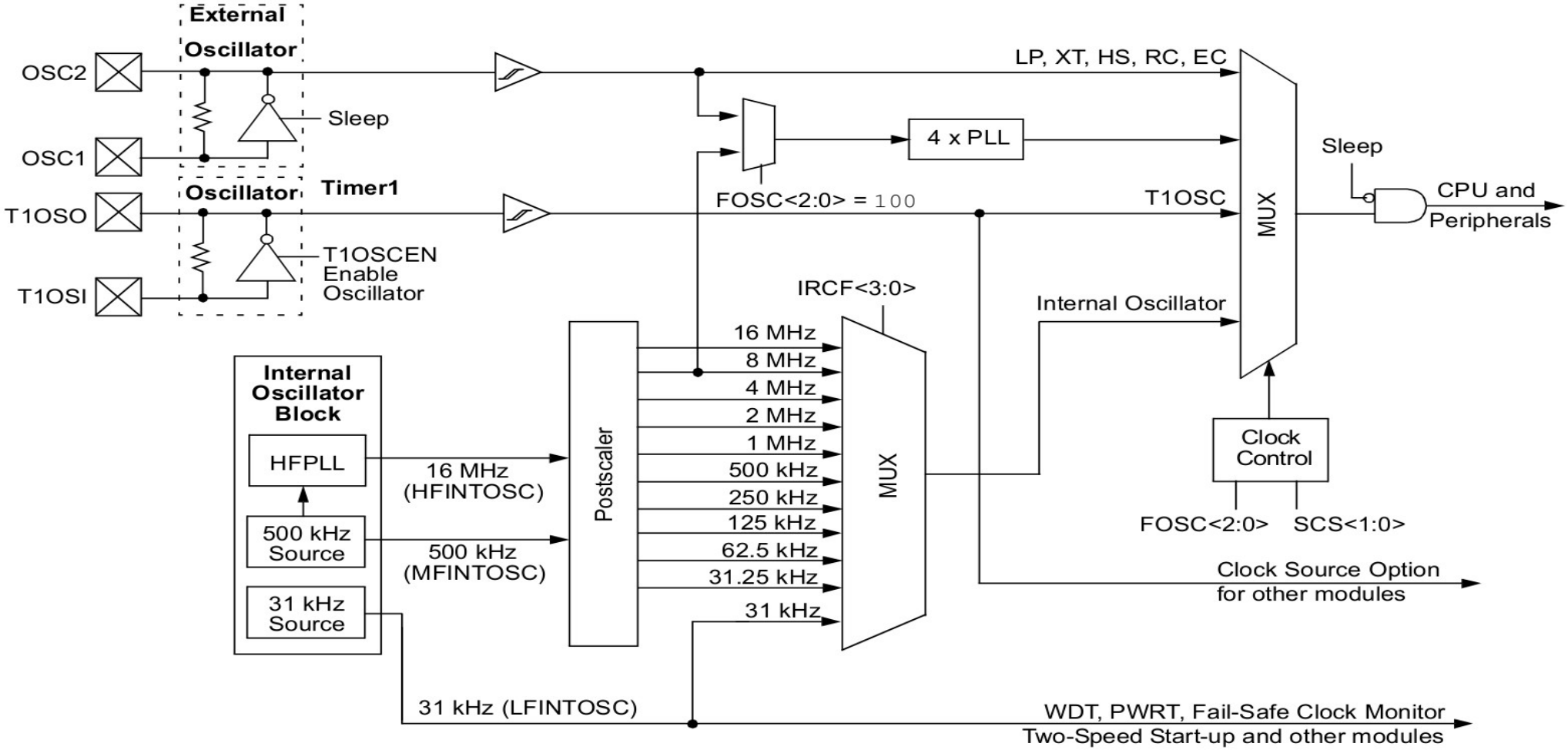


- ADDFSR ***FSRn,k*** → modifica los punteros FSR0 o FSR1
- MOVIW / MOVWF → mueven datos entre W y los registros indirectos INDF0/INDF1

  Distintas posibilidades, por ejemplo para MOVIW (INDFn → W)
  - MOVIW ++INDFn
  - MOVIW --INDFn
  - MOVIW INDFn++
  - MOVIW INDFn--
  - MOVIW k[INDFn] → ofset relativo +k (k entre -32 y +31)
  - MOVIW INDFn
- (instrucciones optimizadas para C)

Oscilador mejorado

- Modos de reloj: EC (externo), LP, XT, HS, RC, INTerno.
- Oscilador interno entre 31Khz y 16Mhz (seleccionable en OSCCON)
- PLL multiplica la Fosc x4 (máximo 32Mhz) → bit PLLEN en la palabra config2 o el bit SPLLEN en el registro OSCCON
- FSCM (Fail-Safe Clock Monitor) → detecta si el reloj (EC,XT,LP,HS,RC) falla y conmuta automáticamente al interno.



REGISTER 5-1: OSCCON: OSCILLATOR CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-1/1	R/W-1/1	R/W-1/1	U-0	R/W-0/0	R/W-0/0
SPLLEN	IRCF<3:0>				—	SCS<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **SPLLEN:** Software PLL Enable bit

If PLLEN in Configuration Word 1 = 1:

SPLLEN bit is ignored. 4x PLL is always enabled (subject to oscillator requirements)

If PLLEN in Configuration Word 1 = 0:

1 = 4x PLL Is enabled

0 = 4x PLL is disabled

bit 6-3 **IRCF<3:0>:** Internal Oscillator Frequency Select bits

000x =31 kHz LF

0010 =31.25 kHz MF

0011 =31.25 kHz HF(1)

0100 =62.5 kHz MF

0101 =125 kHz MF

0110 =250 kHz MF

0111 =500 kHz MF (default upon Reset)

1000 =125 kHz HF(1)

1001 =250 kHz HF(1)

1010 =500 kHz HF(1)

1011 =1 MHz HF

1100 =2 MHz HF

1101 =4 MHz HF

1110 =8 MHz or 32 MHz HF(see **Section 5.2.2.1 "HFINTOSC"**)

1111 =16 MHz HF

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **SCS<1:0>:** System Clock Select bits

1x = Internal oscillator block

01 = Timer1 oscillator

00 = Clock determined by FOSC<2:0> in Configuration Word 1.

Note 1: Duplicate frequency derived from HFINTOSC.

REGISTER 5-2: OSCSTAT: OSCILLATOR STATUS REGISTER

R-1/q	R-0/q	R-q/q	R-0/q	R-0/q	R-q/q	R-0/0	R-0/q
T1OSCR	PLLR	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Conditional

bit 7 **T1OSCR:** Timer1 Oscillator Ready bit

If T1OSCEN = 1:

1 = Timer1 oscillator is ready

0 = Timer1 oscillator is not ready

If T1OSCEN = 0:

1 = Timer1 clock source is always ready

bit 6 **PLLR** 4x PLL Ready bit

1 = 4x PLL is ready

0 = 4x PLL is not ready

bit 5 **OSTS:** Oscillator Start-up Time-out Status bit

1 = Running from the clock defined by the FOSC<2:0> bits of the Configuration Word 1

0 = Running from an internal oscillator (FOSC<2:0> = 100)

bit 4 **HFIOFR:** High Frequency Internal Oscillator Ready bit

1 = HFINTOSC is ready

0 = HFINTOSC is not ready

bit 3 **HFIOFL:** High Frequency Internal Oscillator Locked bit

1 = HFINTOSC is at least 2% accurate

0 = HFINTOSC is not 2% accurate

bit 2 **MFIOFR:** Medium Frequency Internal Oscillator Ready bit

1 = MFINTOSC is ready

0 = MFINTOSC is not ready

bit 1 **LFIOFR:** Low Frequency Internal Oscillator Ready bit

1 = LFINTOSC is ready

0 = LFINTOSC is not ready

bit 0 **HFIOFS:** High Frequency Internal Oscillator Stable bit

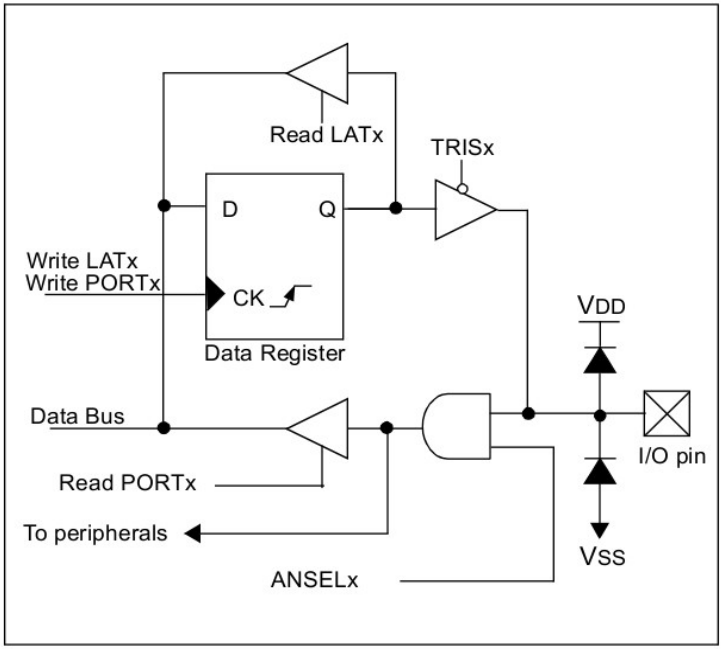
1 = HFINTOSC is at least 0.5% accurate

0 = HFINTOSC is not 0.5% accurate

Puertos (A-E)

- Registros asociados a todos los puertos
  - PORTx, TRISx → igual que antes
  - LATx → evitan problemas con la lectura-modificación-escritura en los puertos
  - APFCON (pag siguiente) → permite cambiar de pin distintas funciones
  - ANSELx → especifico para cada puerto
    - 0=Digital / 1=Analógico
- Interrupciones asociadas a cambio de nivel → PORTB
  - Habilitación individual → dos registros de control
    - IOCBP<7..0> → bit a 1= activada detección flanco subida en ese pin
    - IOCBN<7..0> → bit a 1= detección flanco bajada
  - Registro de flags (IOCBF) → cada bit es un flag
  - INTCON → habilitación: IOCIE + flag global: IOCIF
- Pull-up débil (como entrada)
  - En PORTB completo → registro de control WPUB (bits a 1 → pull-up habilitado en ese pin)
  - En R3 → bit control WPUE3 (registro WPUE)
  - Bit $\overline{\text{WPUEN}}$ (registro option) → a 1 deshabilita todos los pull-up

FIGURE 12-1: GENERIC I/O PORT OPERATION



REGISTER 12-1: APFCON: ALTERNATE PIN FUNCTION CONTROL REGISTER

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	CCP3SEL	T1GSEL	P2BSEL	SRNQSEL	C2OUTSEL	SSSEL	CCP2SEL
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 Unimplemented: Read as '0'.

bit 6 **CCP3SEL**: CCP3 Input/Output Pin Selection bit

For 28-Pin Devices (PIC16F1933/1936/1938):

0 = CCP3/P3A function is on RC6/TX/CK/CCP3/P3A/SEG9
1 = CCP3/P3A function is on RB5/AN13/CPS5/CCP3/P3A/T1G/COM1

For 40-Pin Devices (PIC16F1934/1937/1939):

0 = CCP3/P3A function is on RE0/AN5/CCP3/P3A/SEG21
1 = CCP3/P3A function is on RB5/AN13/CPS5/CCP3/P3A/T1G/COM1

bit 5 **T1GSEL**: Timer1 Gate Input Pin Selection bit

0 = T1G function is on RB5/AN13/CPS5/CCP3/P3A/T1G/COM1
1 = T1G function is on RC4/SDI/SDA/T1G/SEG11

bit 4 **P2BSEL**: CCP2 PWM B Output Pin Selection bit

For 28-Pin Devices (PIC16F1933/1936/1938):

0 = P2B function is on RC0/T1OSO/T1CKI/P2B
1 = P2B function is on RB5/AN13/P2B/CPS5/T1G/COM1

For 40-Pin Devices (PIC16F1934/1937/1939):

0 = P2B function is on RC0/T1OSO/T1CKI/P2B
1 = P2B function is on RD2/CPS10/P2B

bit 3 **SRNQSEL**: SR Latch nQ Output Pin Selection bit

0 = SRnQ function is on RA5/AN4/C2OUT/SRnQ/$\overline{SS}$/CPS7/SEG5/V_{CAP}
1 = SRnQ function is on RA0/AN0/C12IN0-/C2OUT/SRnQ/$\overline{SS}$/SEG12/V_{CAP}

bit 2 **C2OUTSEL**: Comparator C2 Output Pin Selection bit

0 = C2OUT function is on RA5/AN4/C2OUT/SRnQ/$\overline{SS}$/CPS7/SEG5/V_{CAP}
1 = C2OUT function is on RA0/AN0/C12IN0-/C2OUT/SRnQ/$\overline{SS}$/SEG12/V_{CAP}

bit 1 **SSSEL**: $\overline{SS}$ Input Pin Selection bit

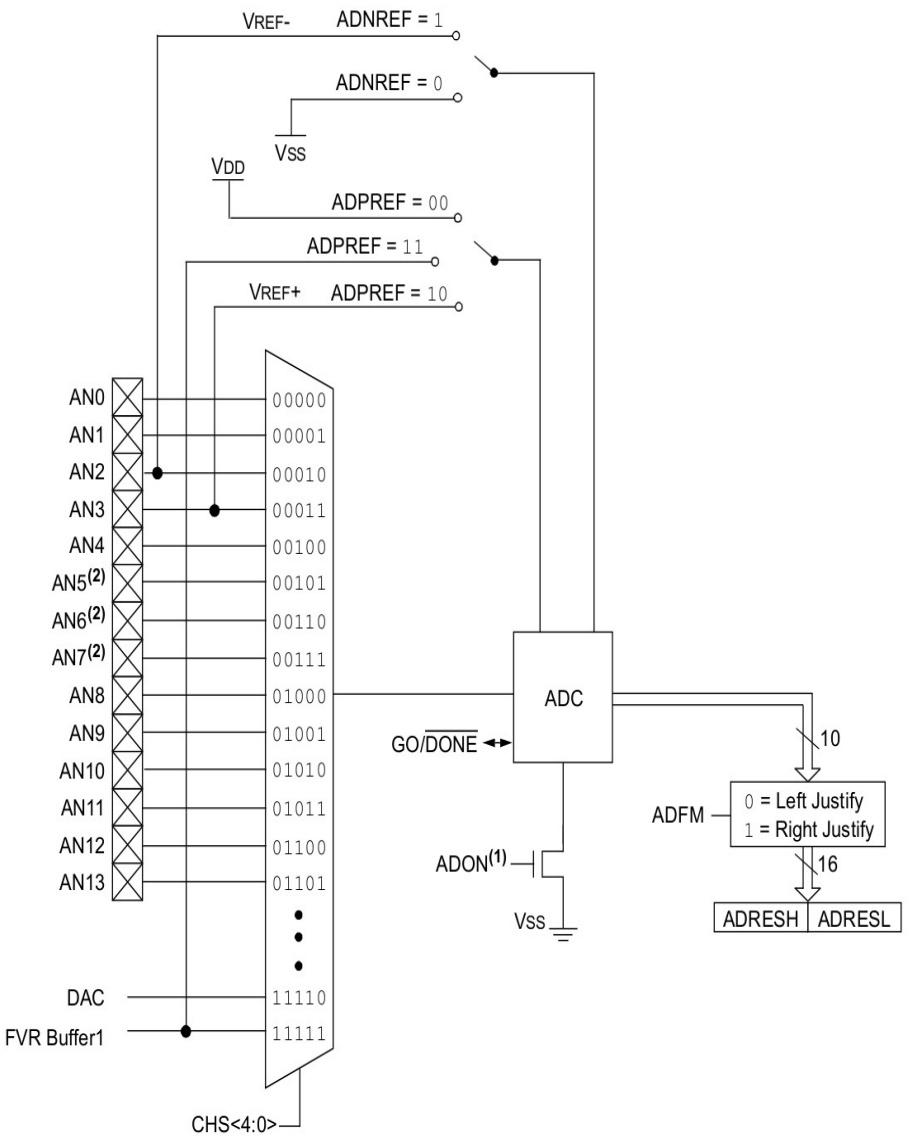
0 = $\overline{SS}$ function is on RA5/AN4/C2OUT/SRNQ/$\overline{SS}$/CPS7/SEG5/V_{CAP}
1 = $\overline{SS}$ function is on RA0/AN0/C12IN0-/C2OUT/SRNQ/$\overline{SS}$/SEG12/V_{CAP}

bit 0 **CCP2SEL**: CCP2 Input/Output Pin Selection bit

0 = CCP2/P2A function is on RC1/T1OSI/CCP2/P2A
1 = CCP2/P2A function is on RB3/AN9/C12IN2-/CPS3/CCP2/P2A/VLCD3

DAC 10 bits

- Casi igual que en PIC16F88
- Mayor número de canales
- Más posibilidades de Vref+ / Vref-
  - Posibilidad de Vref+ desde FVR (referencia de voltaje interna)
  - Configuración de Vraf+ y Vref- con los bits ADNREF Y ADPREF<1..0> de ADCON1
- ¡¡cuidado con la selección de ADCS!! → según la Fosc del micro hay valores de ADCS para los que el ADC no funcionará (tabla15-1)



REGISTER 15-2: ADCON1: A/D CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
ADFM	ADCS<2:0>			—	ADNREF	ADPREF<1:0>	
bit 7							bit 0

bit 2 **ADNREF:** A/D Negative Voltage Reference Configuration bit
- 0 = VREF- is connected to VSS
- 1 = VREF- is connected to external VREF-

bit 1-0 **ADPREF<1:0>:** A/D Positive Voltage Reference Configuration bits
- 00 = VREF+ is connected to VDD
- 01 = Reserved
- 10 = VREF+ is connected to external VREF+
- 11 = VREF+ is connected to internal fixed voltage reference

Note 1: When ADON = 0, all multiplexer inputs are disconnected.
2: Not available on PIC16F/LF1933/1936/1938.

FVR

EUSART

CCP/ECCP

Timers

Módulo sensor capacitivo

Módulo de control de LCD

Latch SR