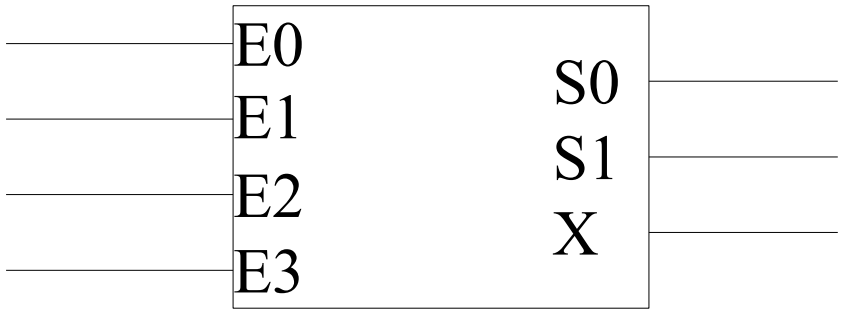
Sistemas combinacionales

- Cada salida es función de una o más entradas
- Las salidas cambian con las entradas

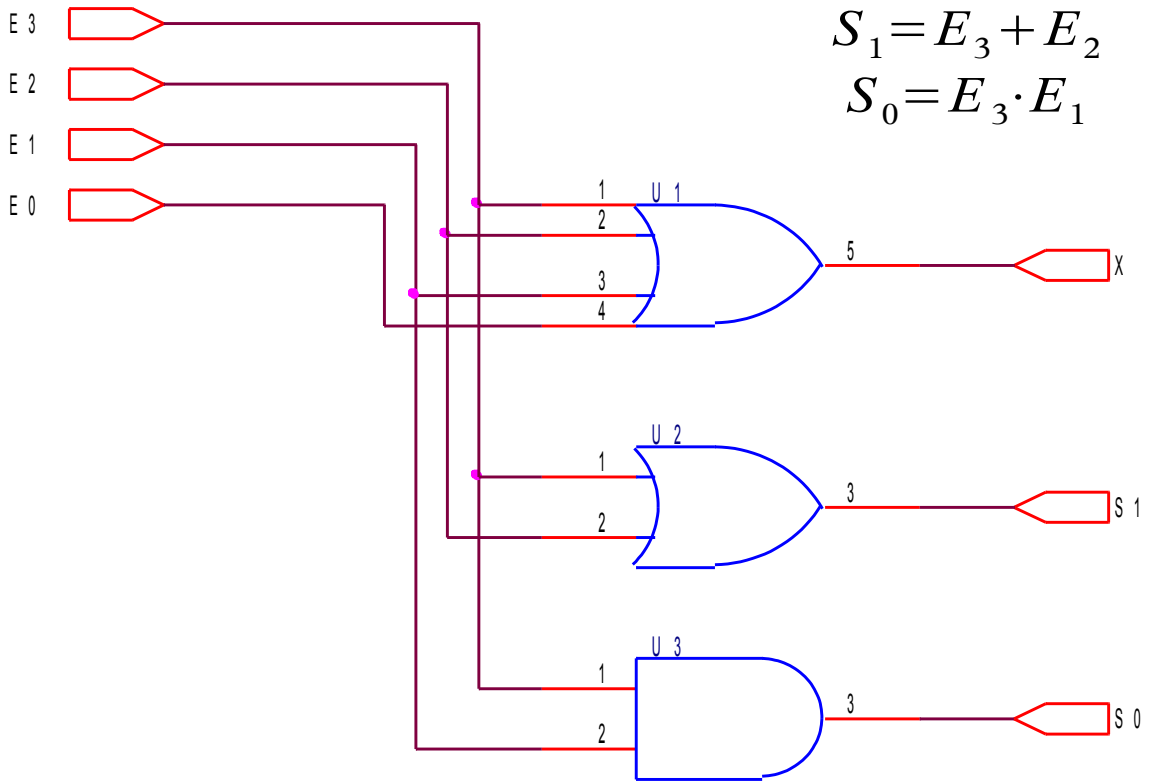
entradas				salidas		
E3	E2	E1	E0	S1	S0	X
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	1
0	0	1	1	0	1	1
0	1	0	0	1	0	1
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	1	0	1
1	0	0	0	1	1	1
1	0	0	1	1	1	1
1	0	1	0	1	1	1
1	0	1	1	1	1	1
1	1	0	0	1	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1



$$X = E_3 + E_2 + E_1 + E_0$$

$$S_1 = E_3 + E_2$$

$$S_0 = E_3 \cdot E_1$$

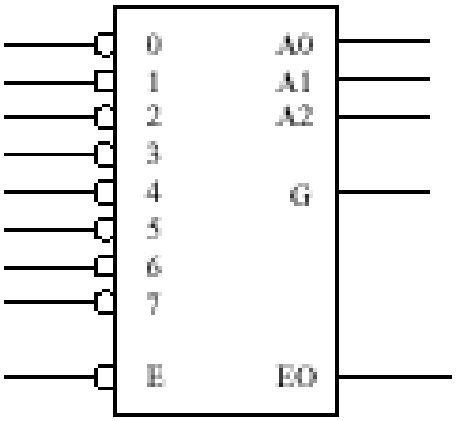


Convenios para entradas y salidas

$\overline{A}$
$\overline{B}$ } Activas a Nivel Bajo (cero lógico)
$\overline{C}$

D
E } Activas a Nivel Alto (uno lógico)
F

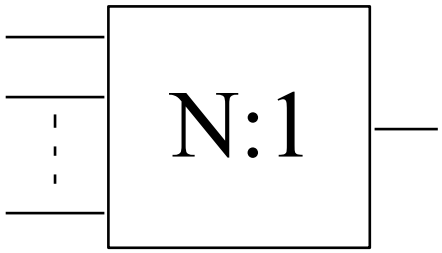
representación

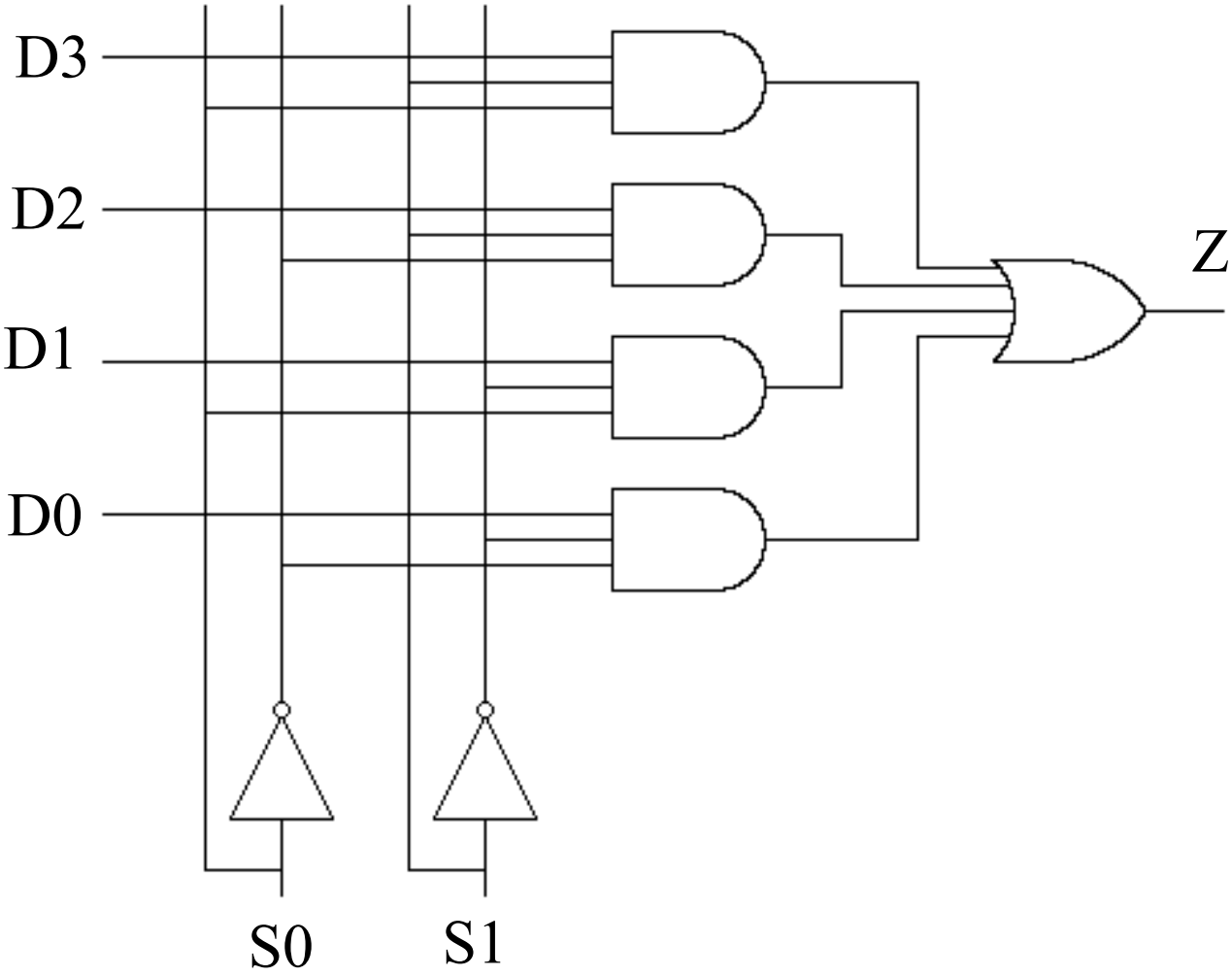


ENABLE = habilita las salidas

DISABLE = inhibe las salidas

Multiplexores





APLICACIONES

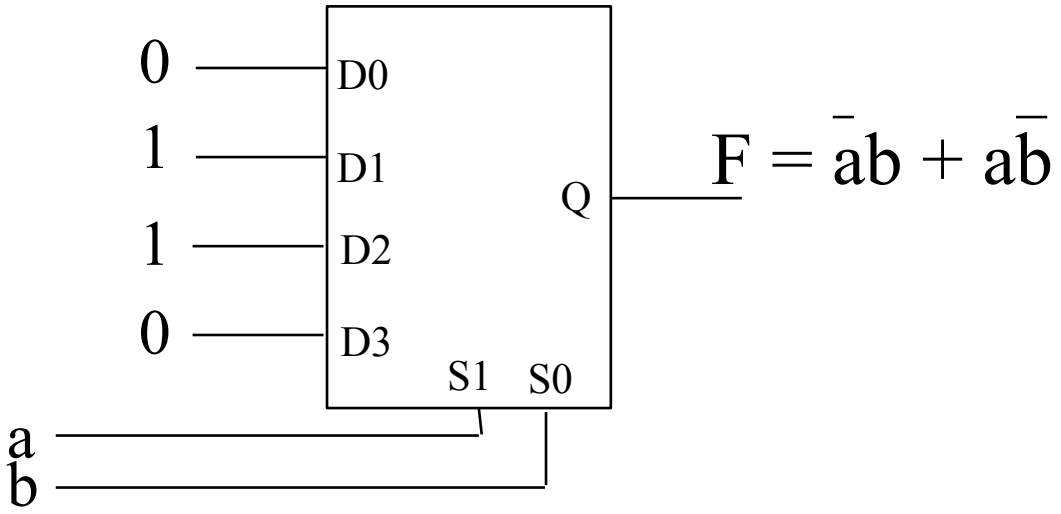
- Selector de datos
- Realización de funciones lógicas
- Multiplexación de señales en el tiempo

$$Z = D_0\overline{S_0}\,\overline{S_1} + D_1 S_0\overline{S_1} + D_2\overline{S_0} S_1 + D_3 S_0 S_1$$

Realización de funciones lógicas con multiplexores

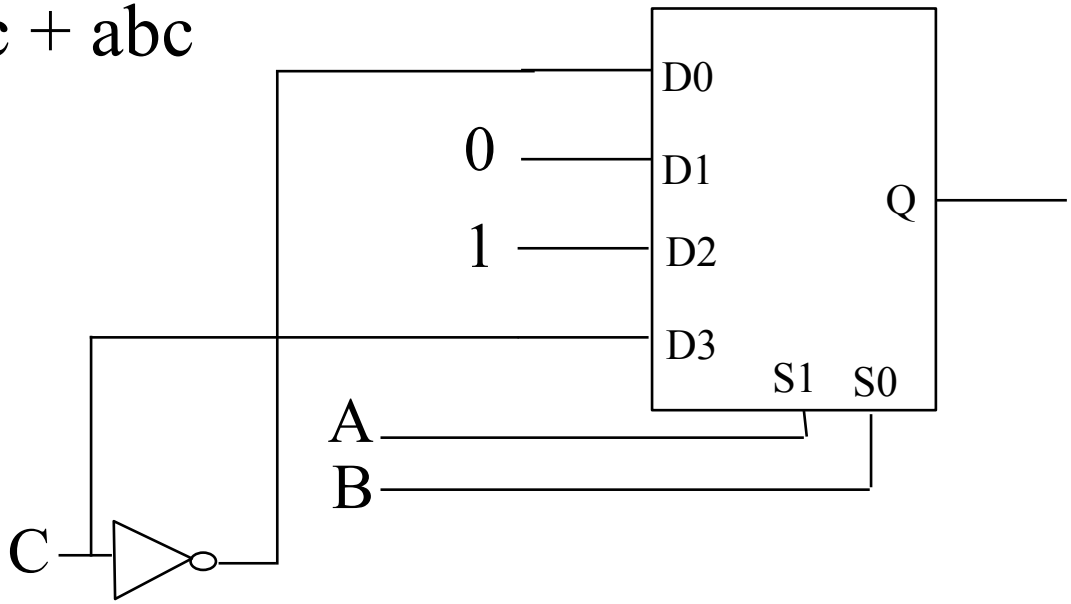
$F = \bar{a}b + a\bar{b}$

a b	F
00	0
01	1
10	1
11	0

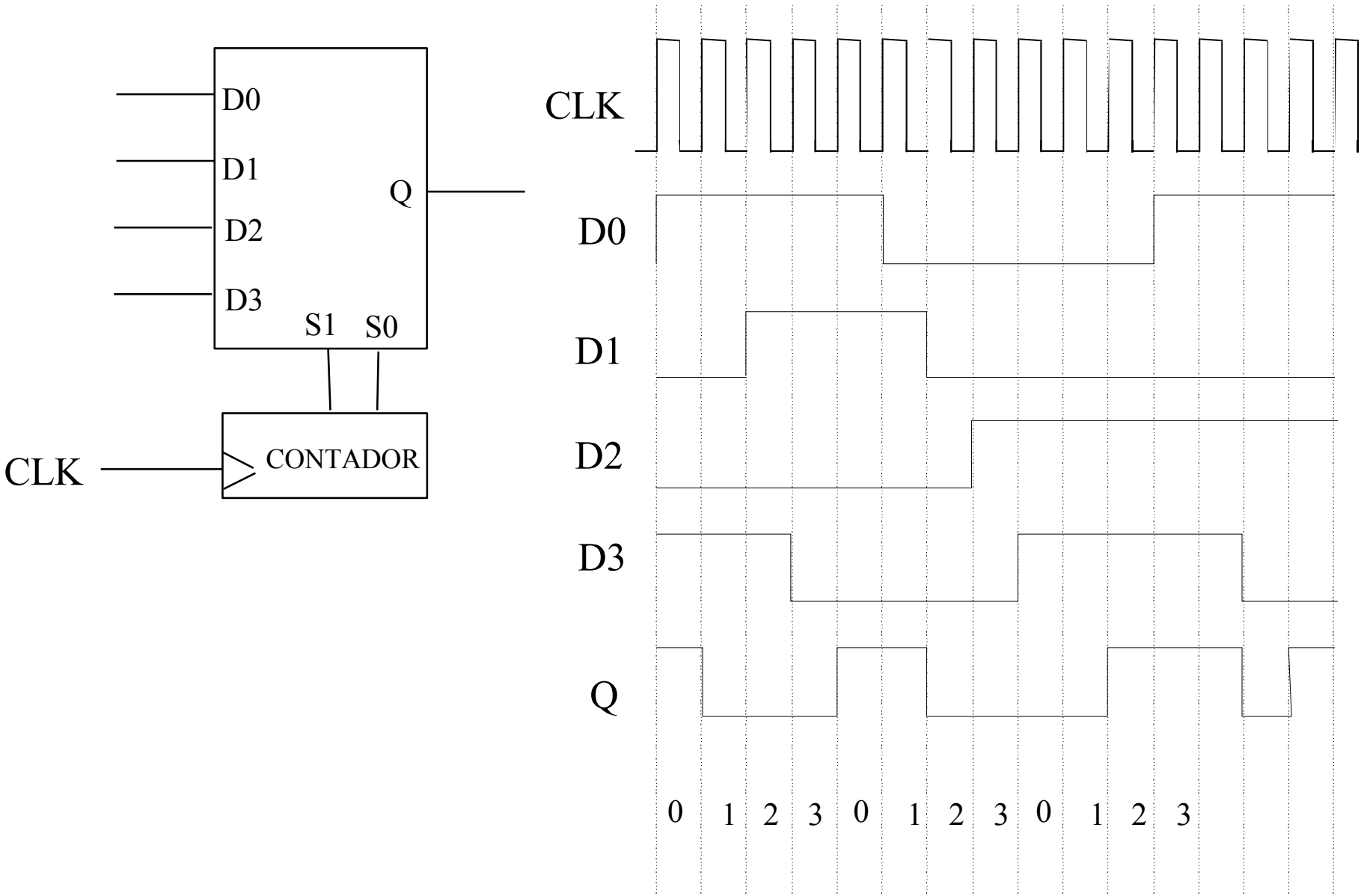


$F = \bar{a}\bar{b}\bar{c} + a\bar{b}\bar{c} + a\bar{b}c + abc$

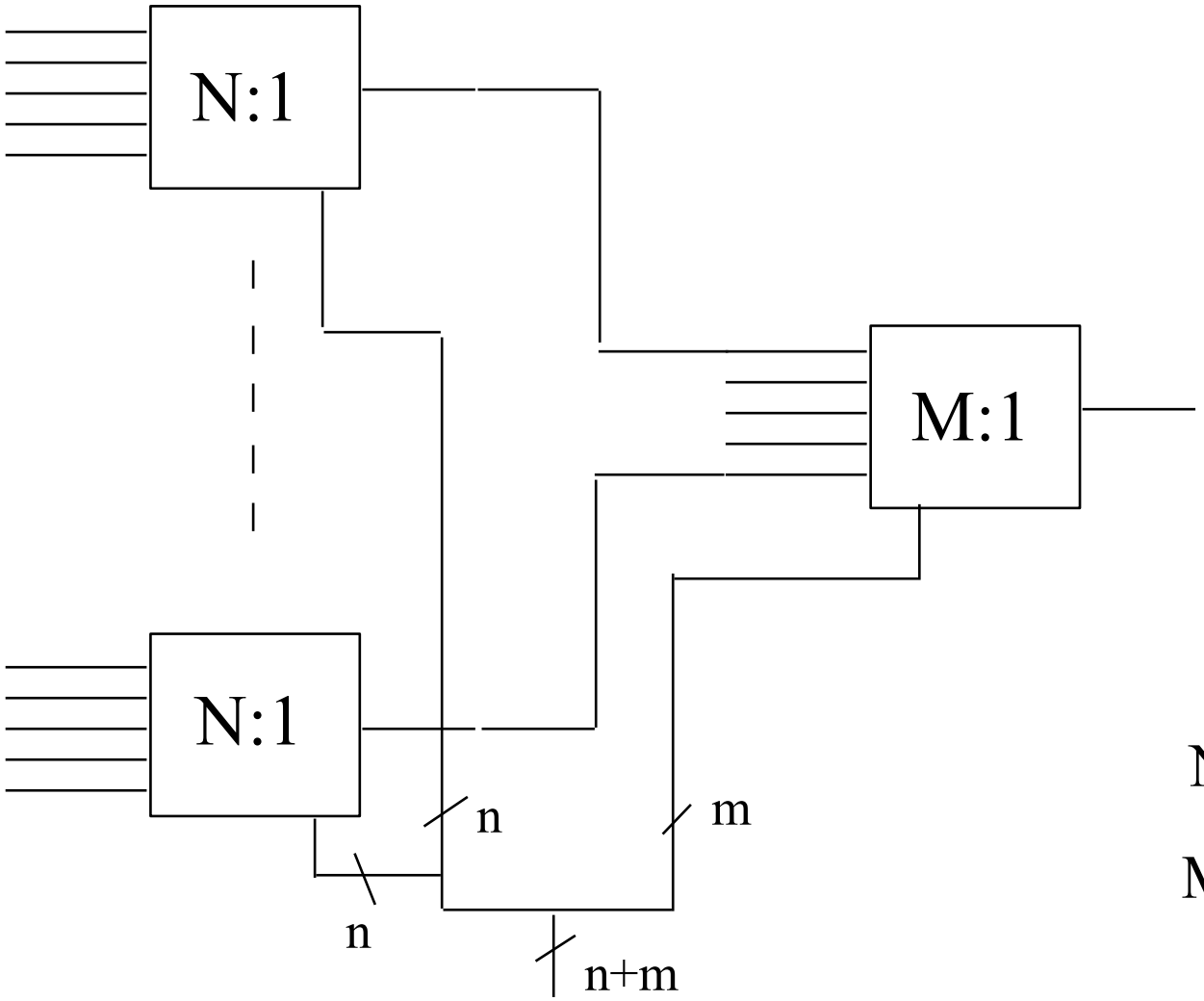
a b c	F
000	1
001	0
010	0
011	0
100	1
101	1
110	0
111	1



Multiplexación en el tiempo



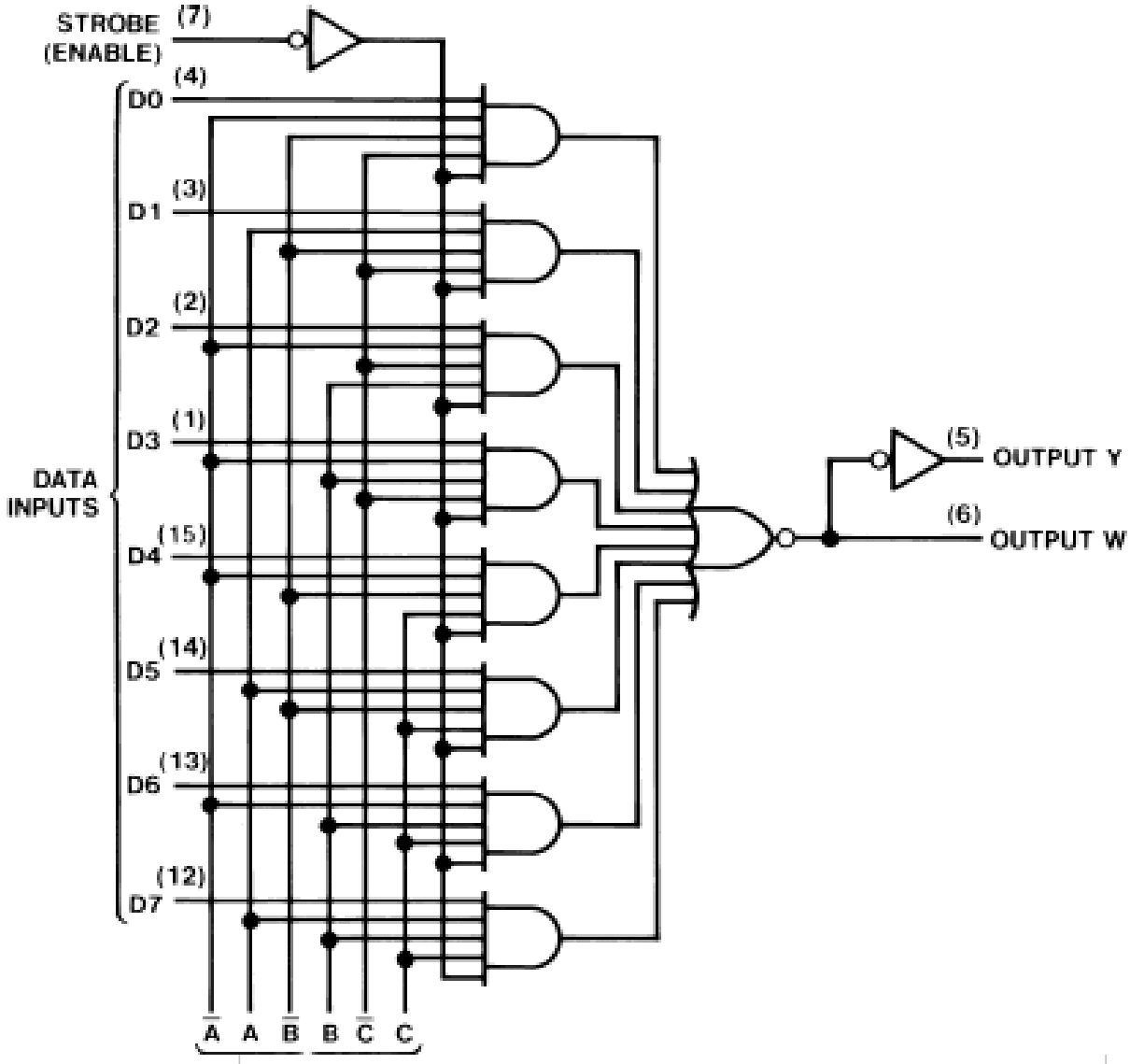
Extensión de multiplexores



$$N = 2^{n}$$

$$M = 2^{m}$$

LS151

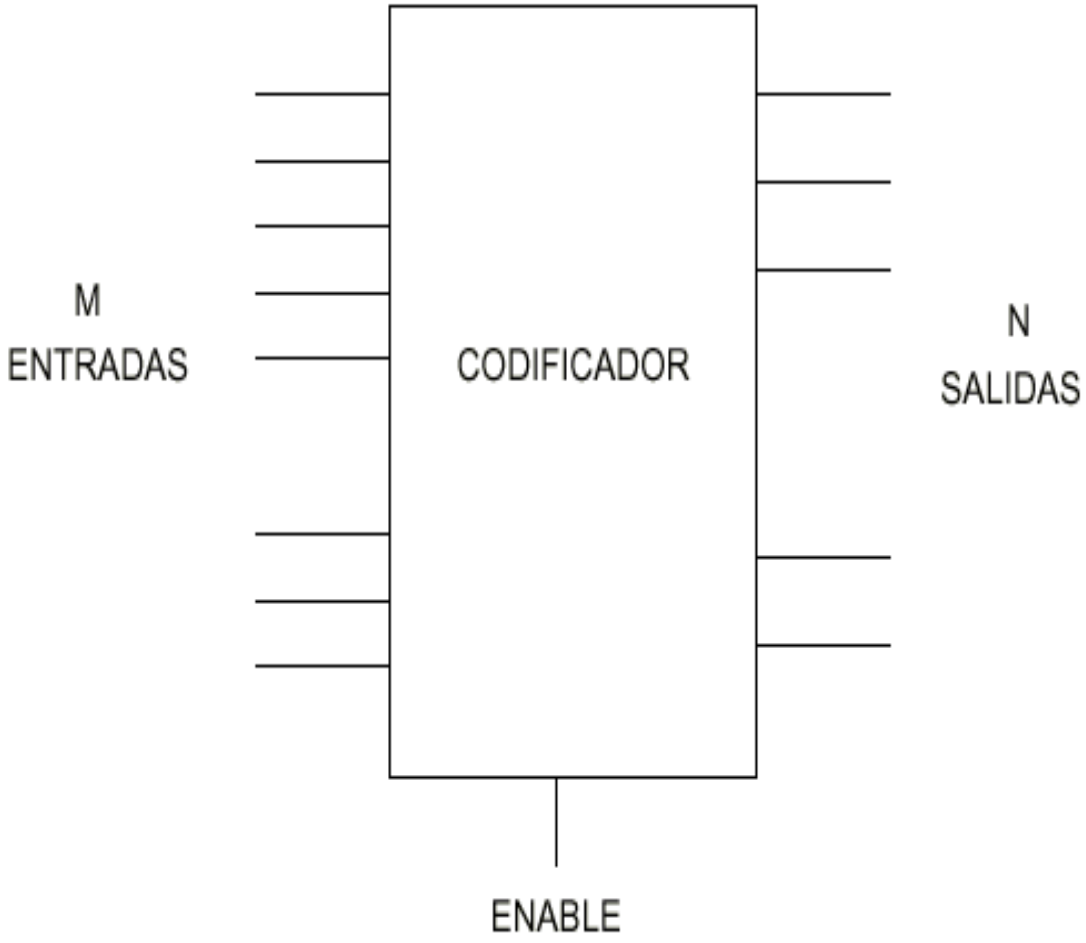


Inputs				Outputs	
Select			Strobe	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care
D0, D1...D7 = the level of the respective D input

Codificadores

EXCITANDO UNA ENTRADA SE GENERA UN CODIGO DE N BITS EN LAS SALIDAS



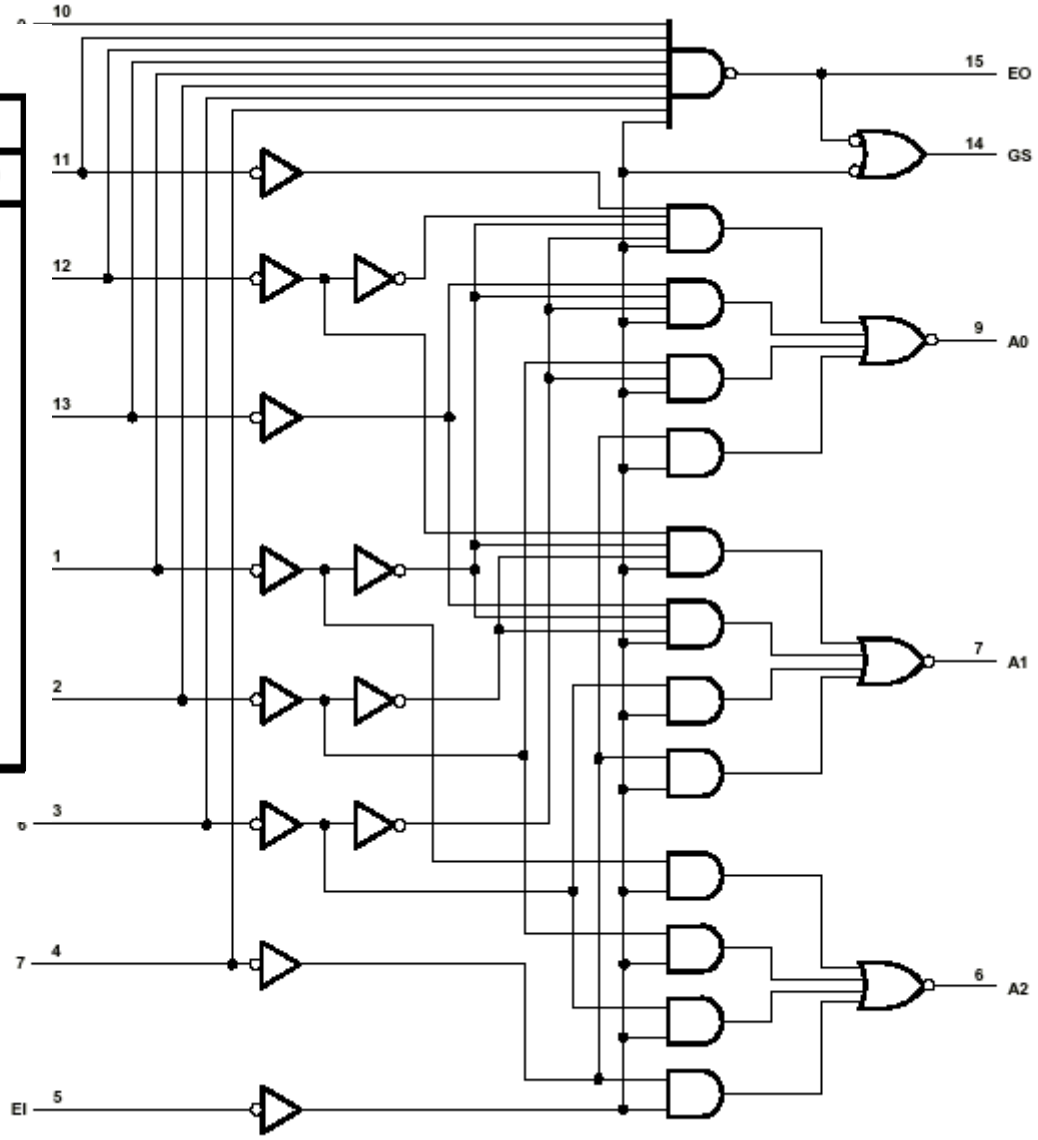
$$M \leq 2^N$$

Tipos:
Con prioridad
Sin Prioridad

Codificador 8 a 3 con prioridad74148

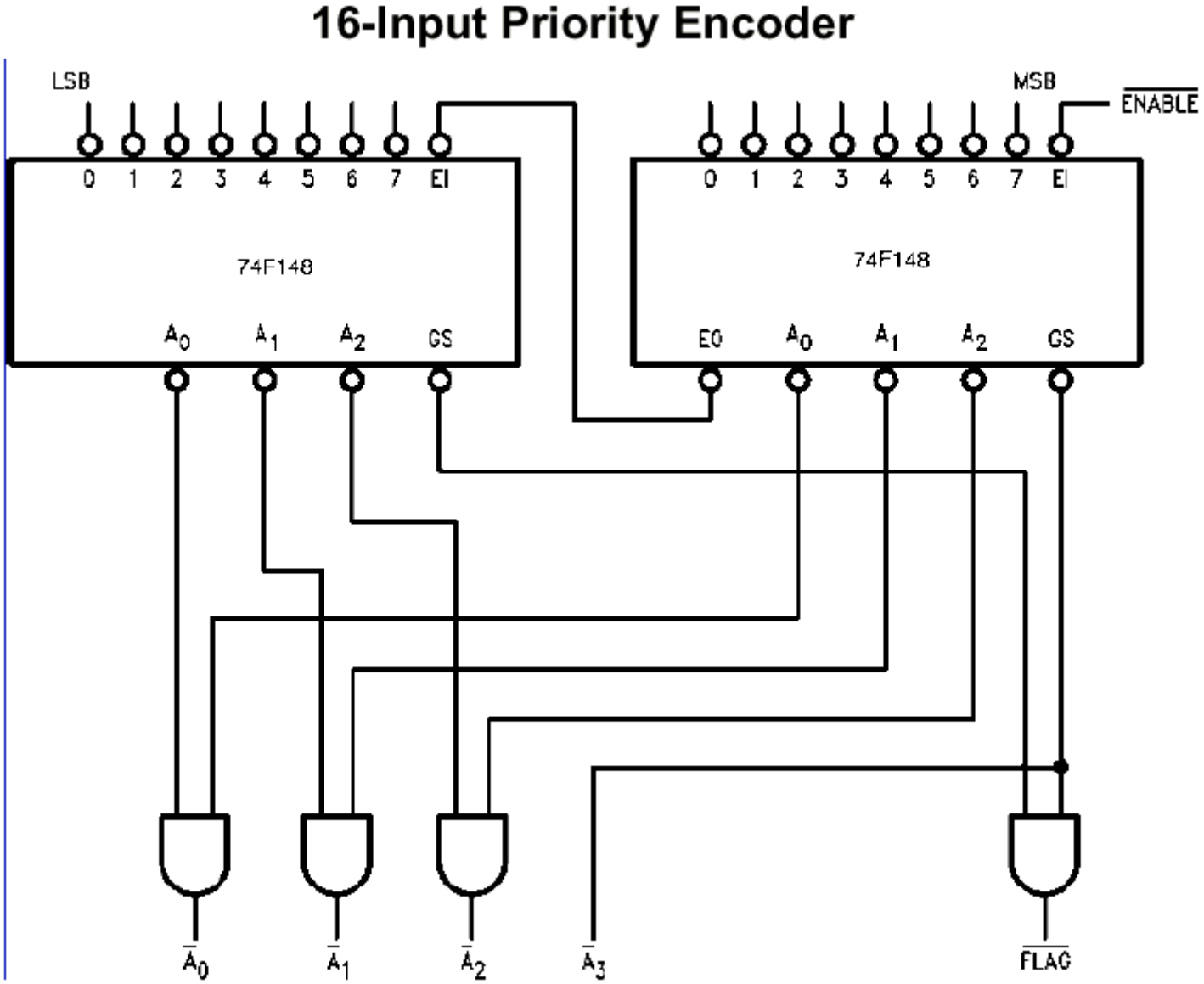
FUNCTION TABLE

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H



EI = entrada ENABLE
GS= señal de grupo
EO= salida ENABLE

Extensión de codificadores



Salidas

A0..A2 = código de la entrada activada en un 148

A3 = activa si se ha activado una entrada en el 2º 148

Demultiplexores

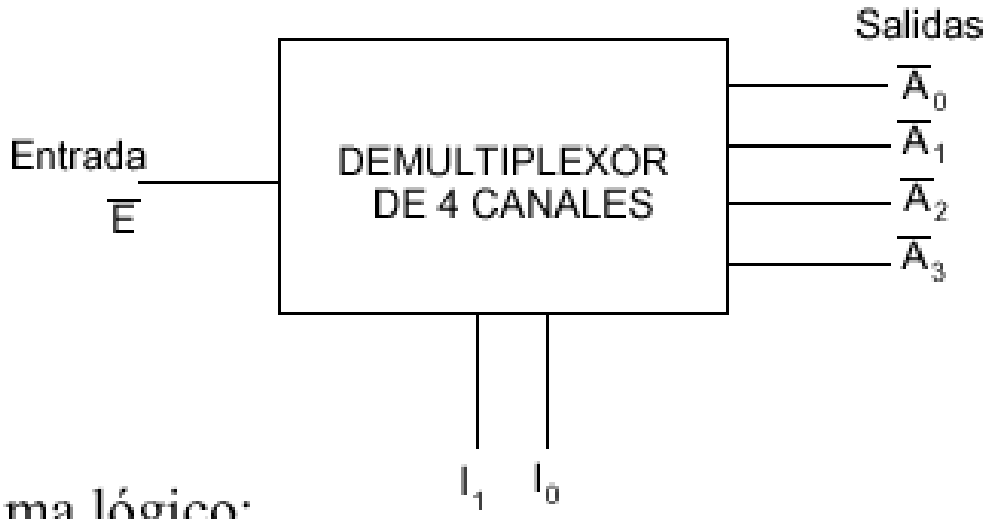


Diagrama lógico:

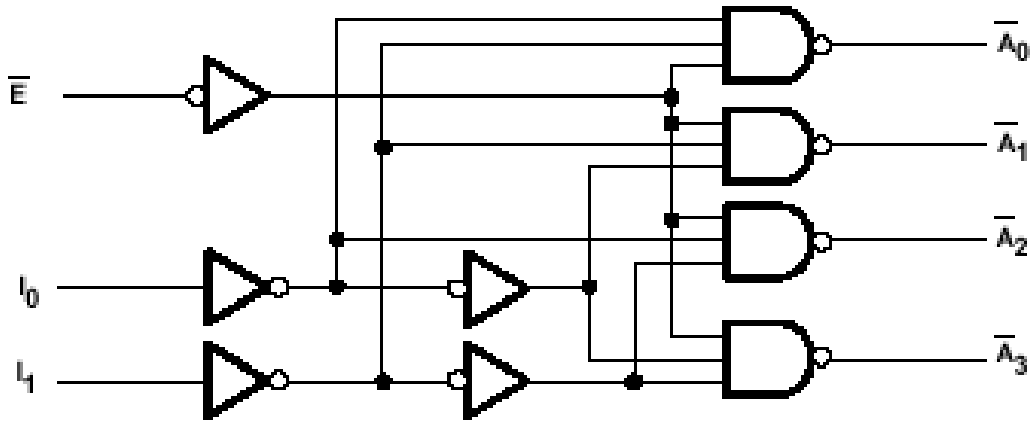


Tabla de funcionamiento:

$\overline{E}$	I_1	I_0	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

Decodificadores

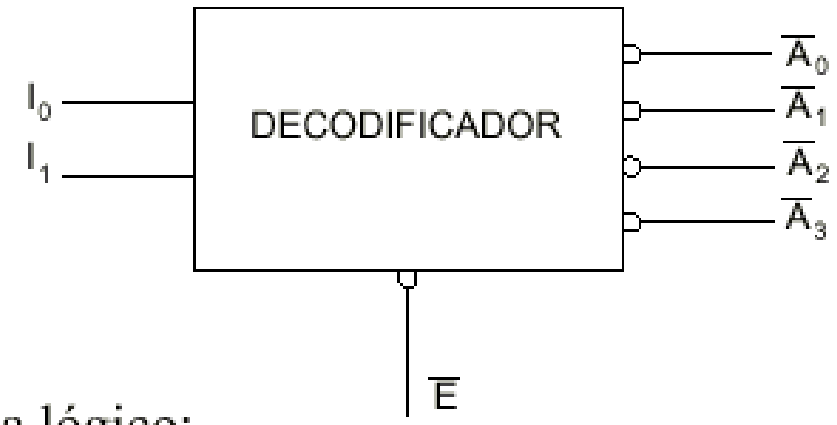


Diagrama lógico:

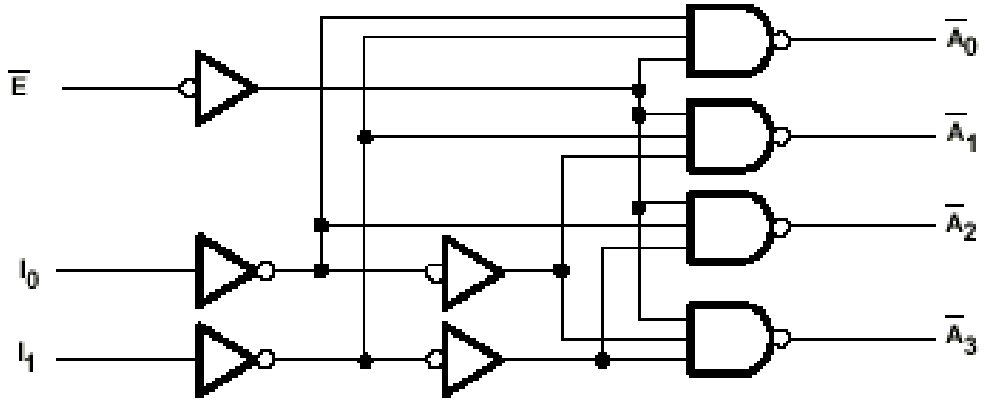


Tabla de funcionamiento:

$\overline{E}$	I_1	I_0	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

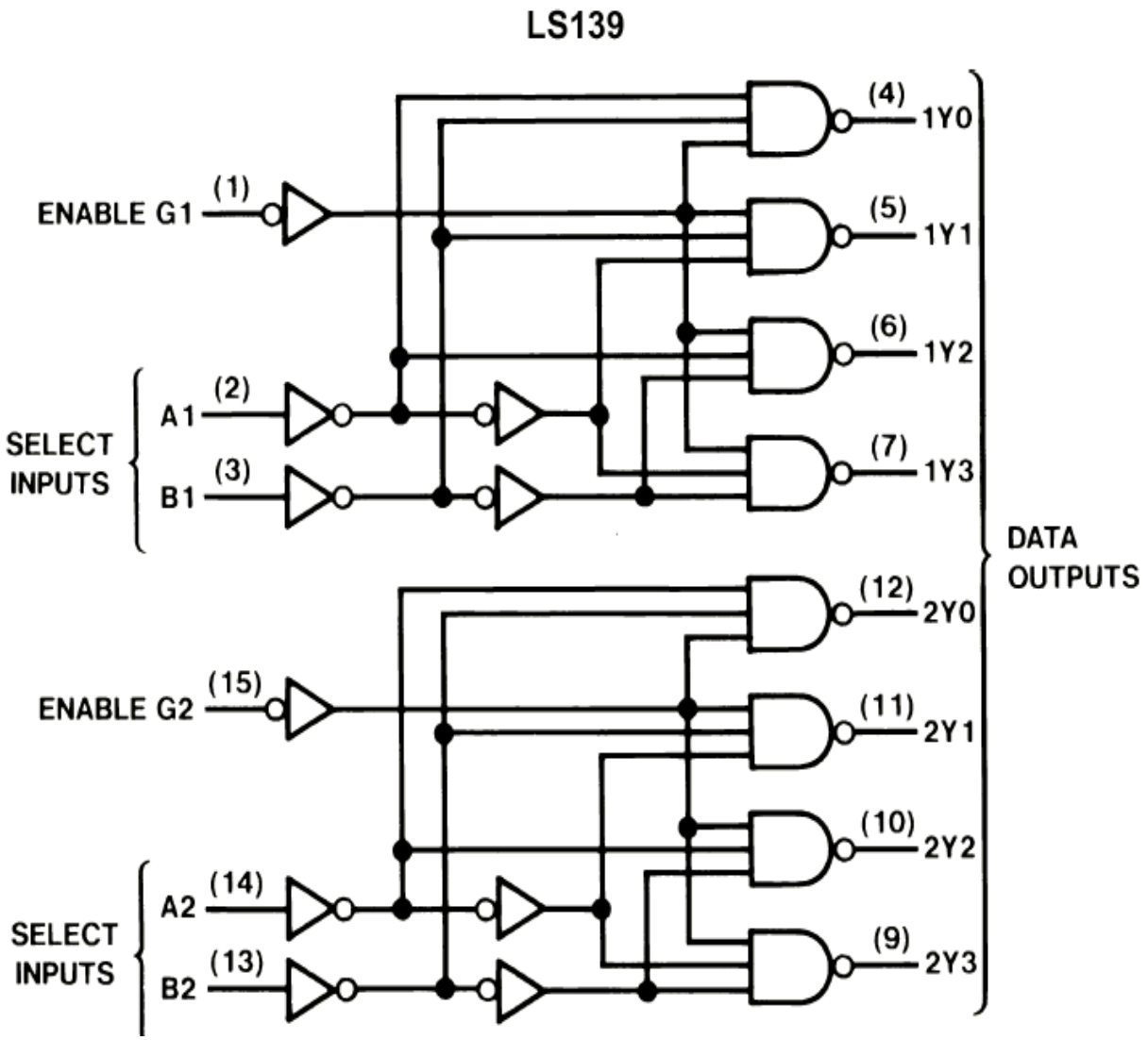
Sólo una salida activa a la vez

Doble decodificador/demultiplexor 2 a 4 74139

LS139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = High Level, L = Low Level, X = Don't Care



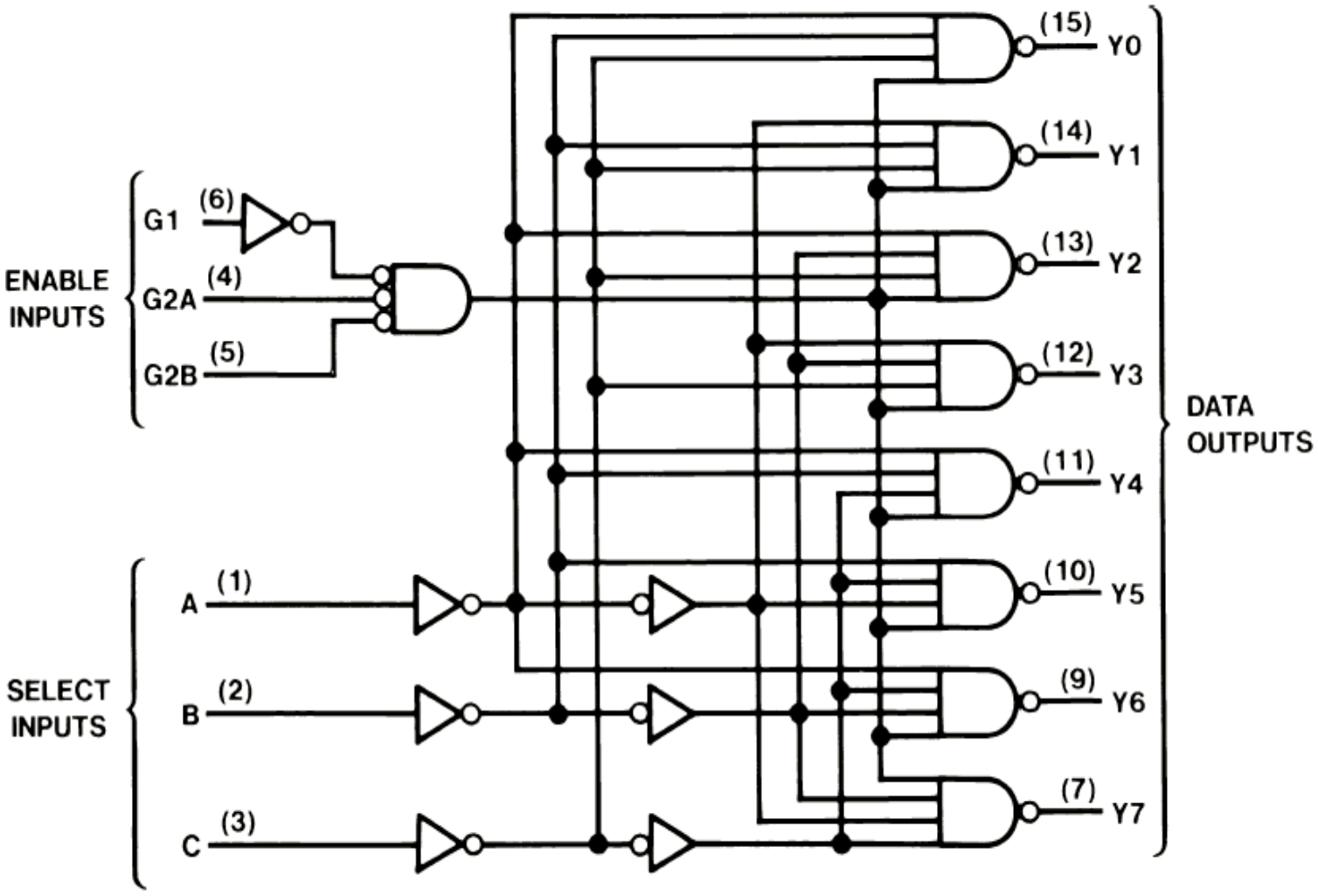
Decodificador/demultiplexor 3 a 8 74138

LS138

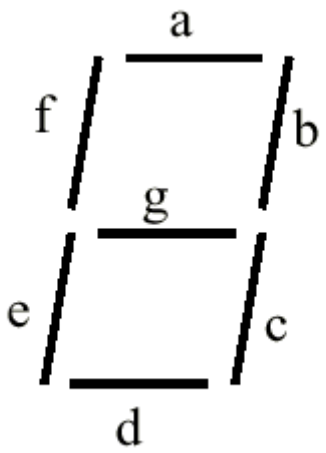
Inputs					Outputs							
Enable		Select										
G1	G2 (Note 8)	C	B	A	YO	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

H = High Level, L = Low Level, X = Don't Care

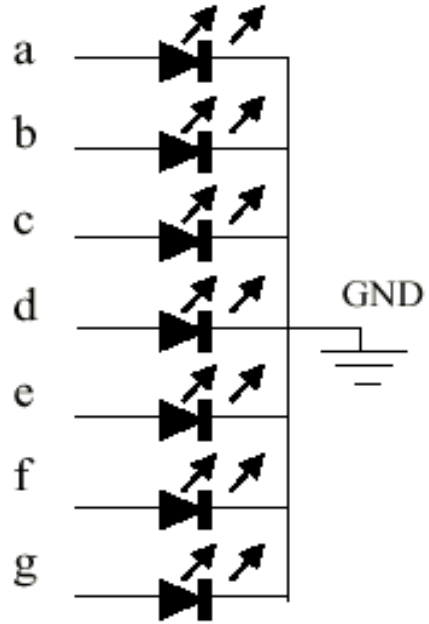
Note 8: G2 = G2A + G2B



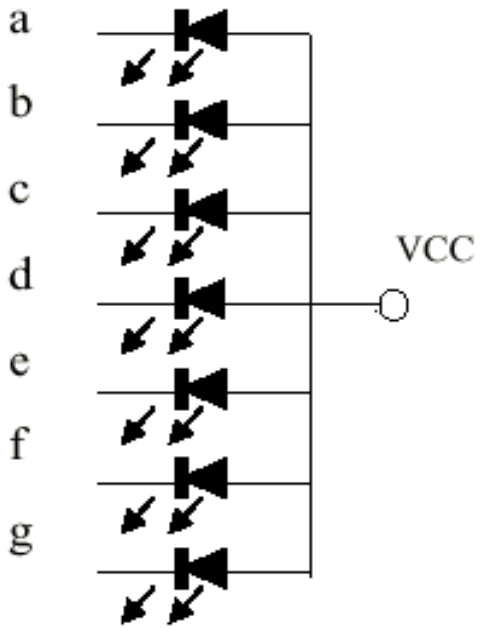
Decodificadores-excitadores BCD-7 segmentos



Activa varias salidas a la vez
Entrega corriente para excitar los led
Cátodo común: salidas activas a nivel alto
Ánodo común: salidas activas a nivel bajo



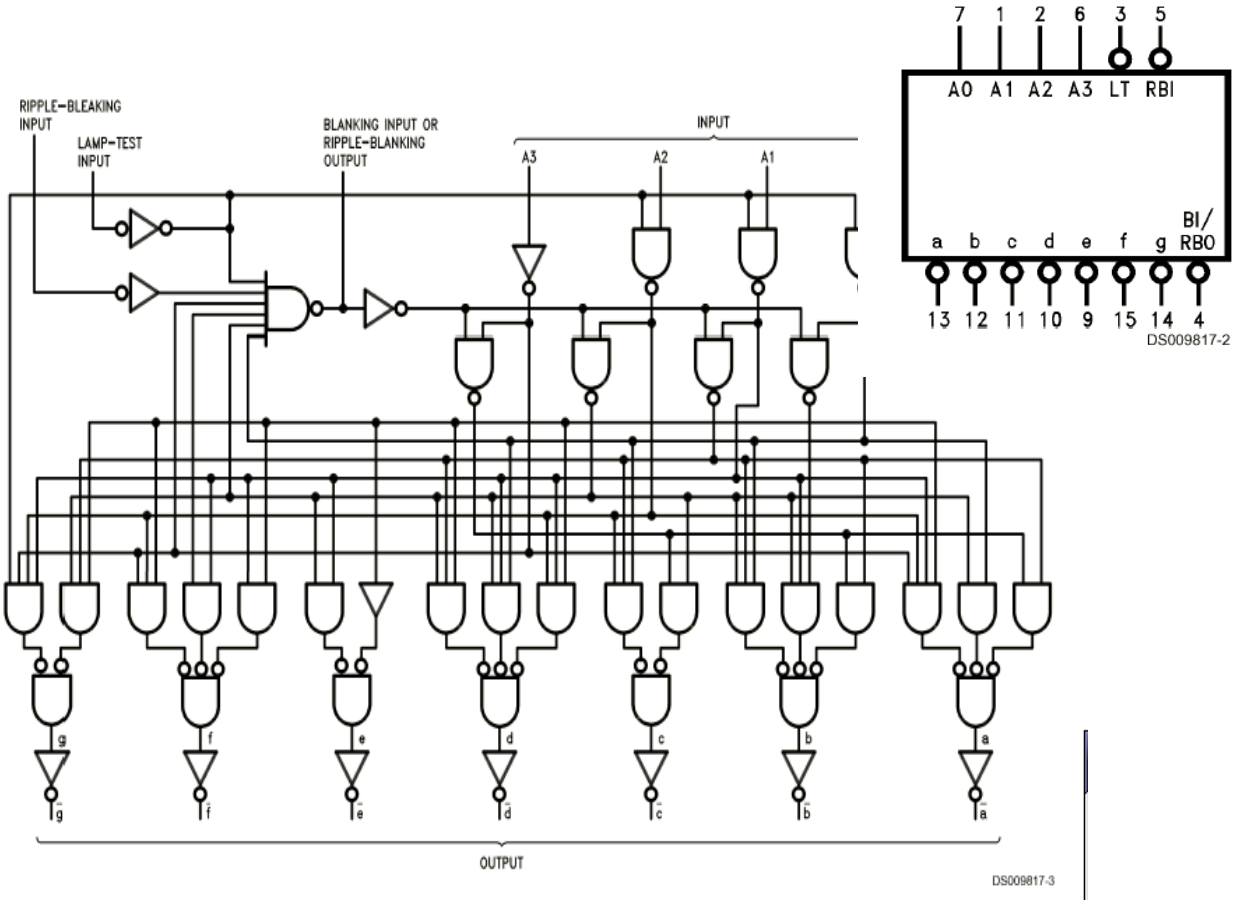
CÁTODO COMÚN

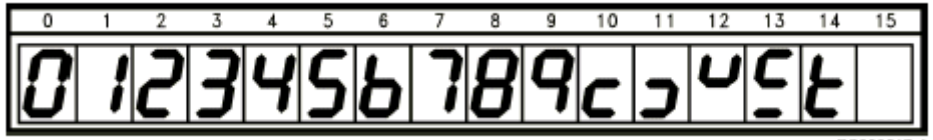


ÁNODO COMÚN

LT	RBI	BI/RBO	A3..A0	Funcionamiento
LT	X	H (salida)	Indif	Se encienden todos
X	X	L (entrada)	Indif	Se apagan todos
H	L	L (salida)	LLLL	Se apagan todos
H	X	H (salida)	Cualquiera menos LLLL	Normal
H	H	H (salida)	LLLL	Aparece el 0

LT=LAMP TEST
RBI=RIPPLE BLANKING INPUT
BI/RBO=BLANKING INPUT/RIPPLE BLANKING OUTPUT





DS009817-4

Decimal or Function	Inputs							Outputs							Note
	$\overline{LT}$	$\overline{RBI}$	A3	A2	A1	A0	$\overline{BI/RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	(Note 7)
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	(Note 7)
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(Note 8)
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(Note 9)
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(Note 10)

Note 7: $\overline{BI/RBO}$ is wire-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking or a decimal 0 is not desired. X = input may be HIGH or LOW.

Note 8: When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a HIGH level regardless of the state of any other input condition.

Note 9: When ripple-blanking input ($\overline{RBI}$) and inputs A0, A1, A2 and A3 are LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

Note 10: When the blanking input/ripple-blanking output ($\overline{BI/RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

Generadores/comprobadores de paridad

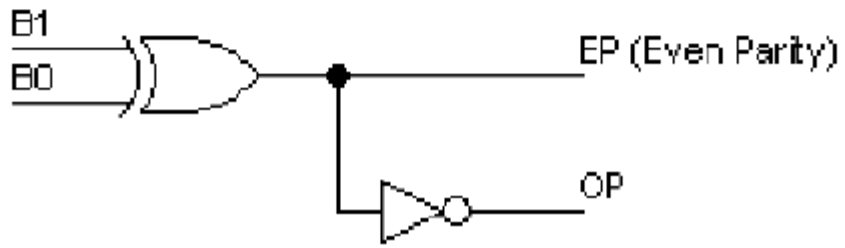
B1	B0	EP	OP
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

EP: PARIDAD PAR

OP: PARIDAD IMPAR

$$EP = \overline{B1}.B0 + B1.\overline{B0} = B1 \oplus B0$$

$$OP = \overline{EP}$$

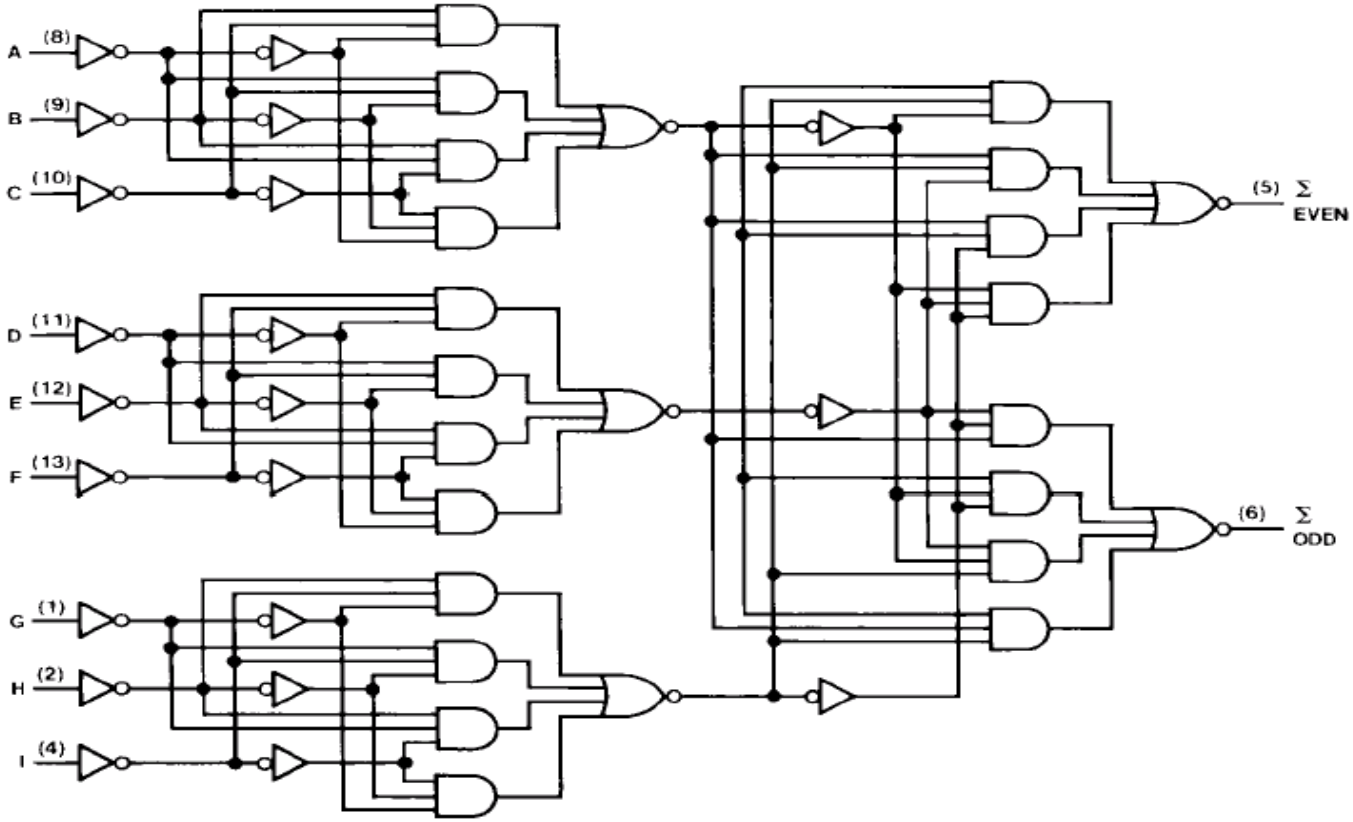


74280 Generador de paridad de 9 bits

Function Table

Number of Inputs (A Thru I) that are HIGH	Outputs	
	∑ Even	∑ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

Logic Diagram



Comparadores

A	B	E	G	L
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

A, B: Entradas

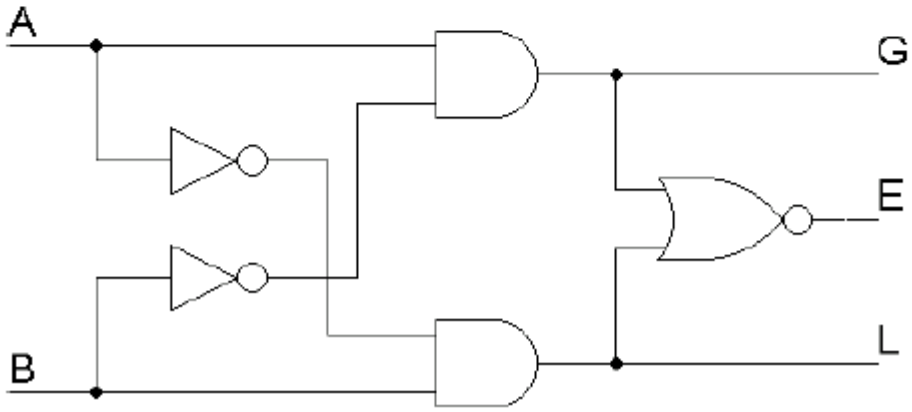
E: Salida de igualdad (A = B)

G: Salida que indica A > B

L: Salida que indica A < B

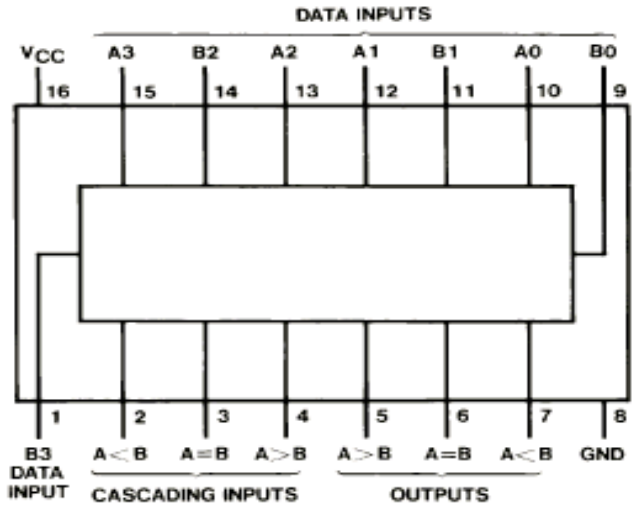
$G = A.\overline{B}$ $\quad L = \overline{A}.B$

$E = \overline{G + L}$



Comparador de 4 bits 7485

Dual-In-Line Package



TL/F/6379–1

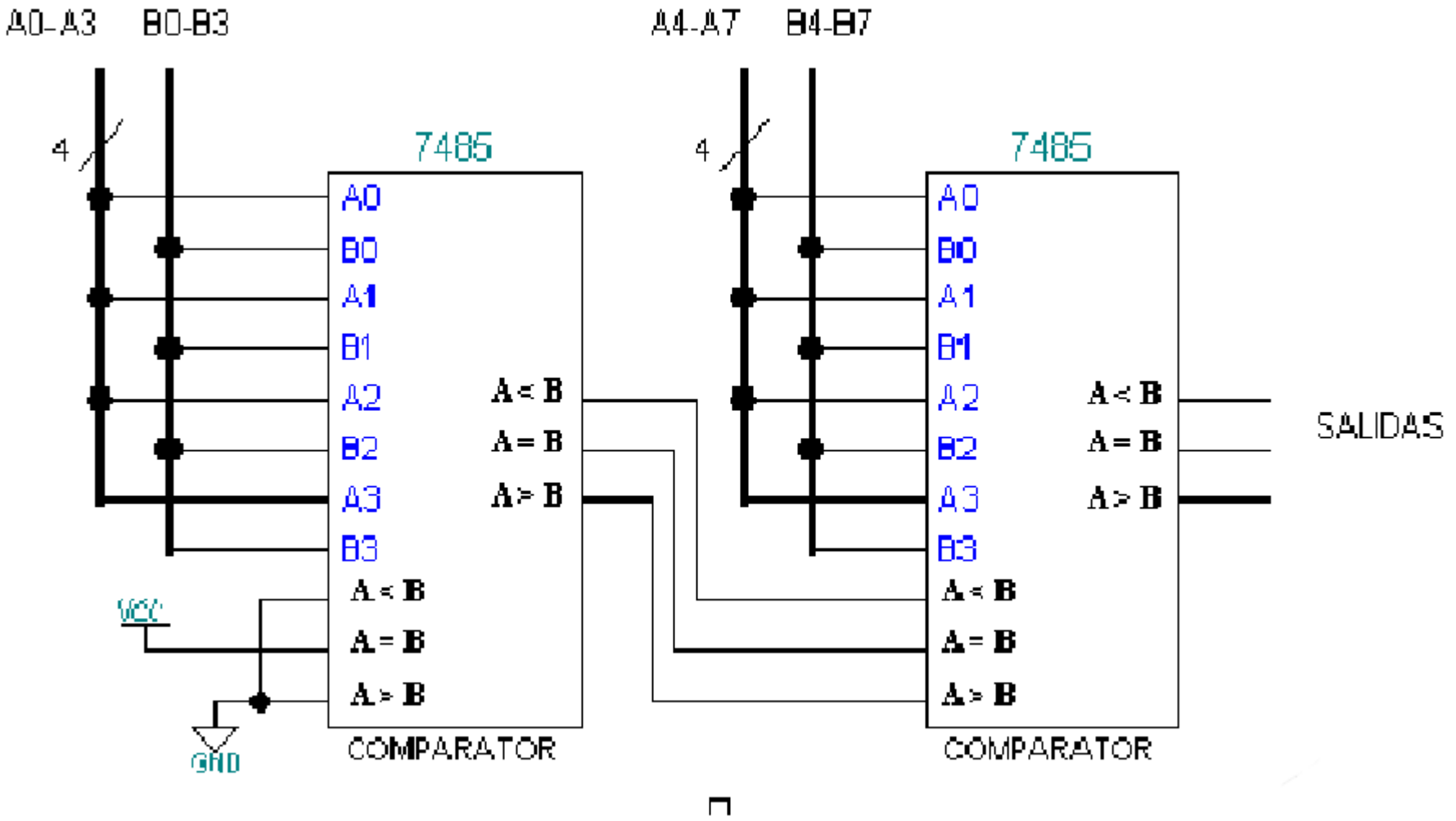
Order Number 54LS85DMQB, 54LS85FMQB, 54LS85LMQB, DM54LS85J, DM54LS85W, DM74LS85M or DM74LS85N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

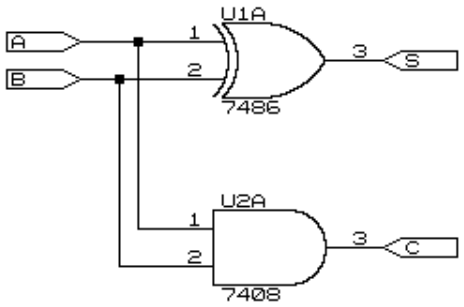
Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

H = High Level, L = Low Level, X = Don't Care

Extensión de comparadores

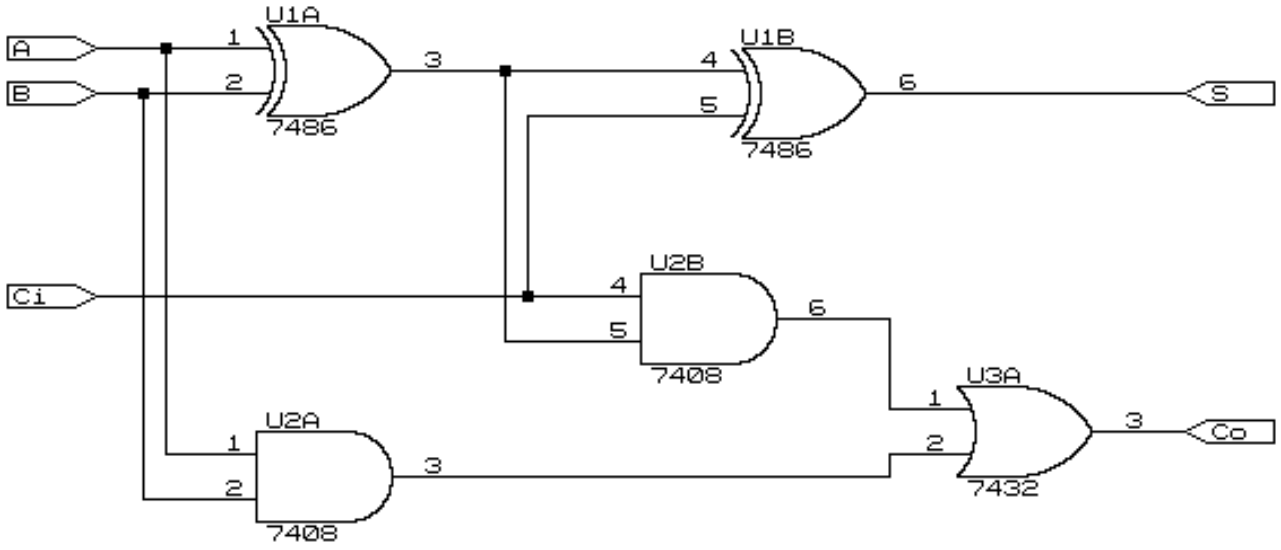


Sumadores



A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

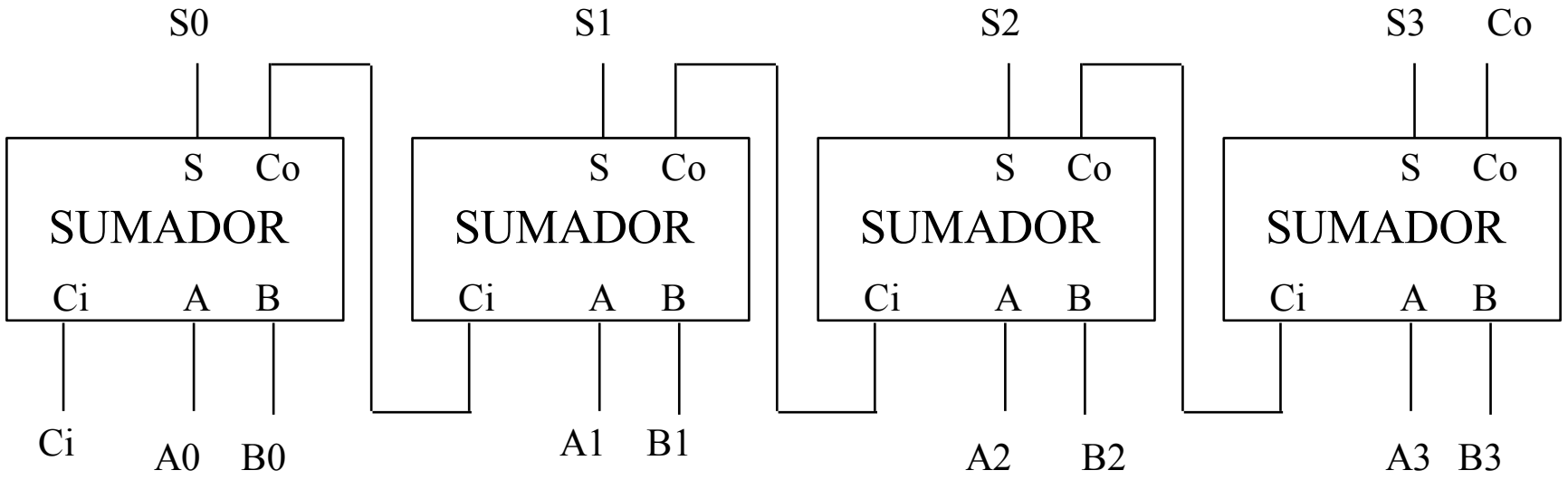
$S = A \oplus B$ $C = AB$



$S = A \oplus B \oplus C$ $Co = AB + (A \oplus B)Ci$

A	B	Ci	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Sumador paralelo con acarreo serie



Tsuma_total = Tsuma * N

Sumador con acarreo anticipado

$Si = Ai \oplus Bi \oplus Ci$

$C_{i+1} = A_iB_i + (A_i \oplus B_i)C_i \quad = \quad G_i + P_iC_i$

$G_i = A_iB_i$ -> acarreo generado

$P_i = A_i \oplus B_i$ -> acarreo propagado

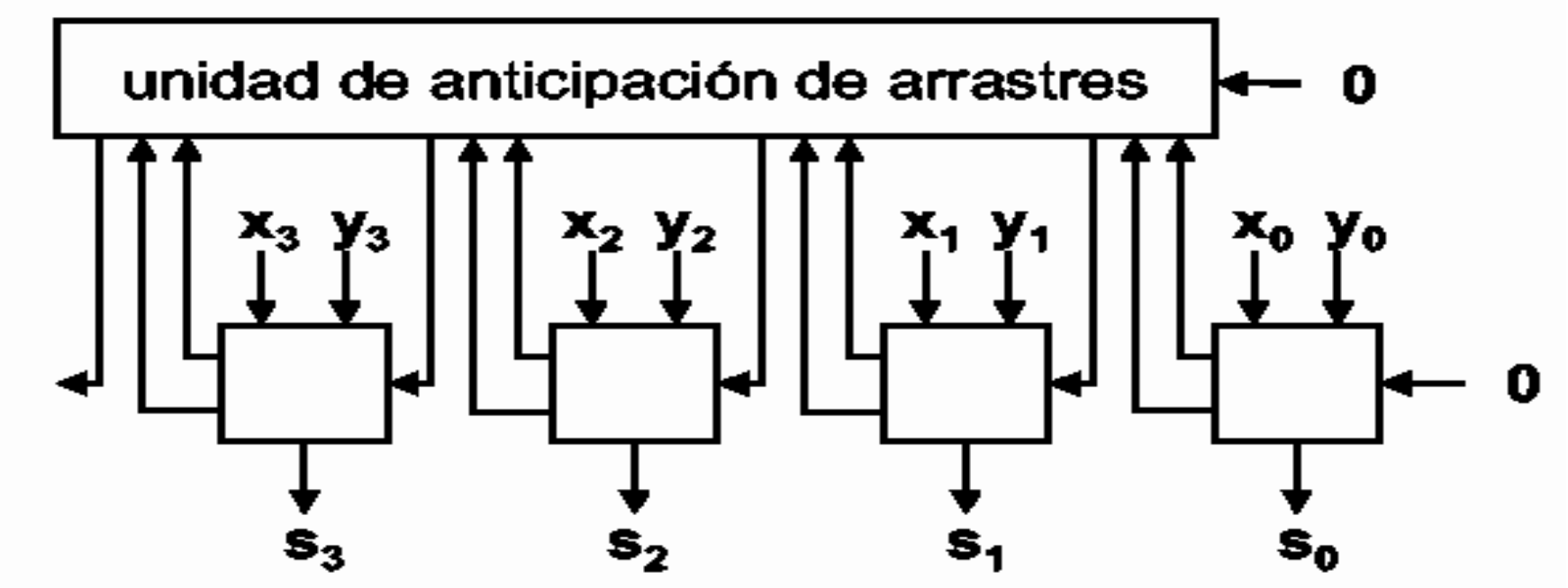
$$c_1 = G_0 + P_0 \cdot c_0$$

$$c_2 = G_1 + P_1 \cdot c_1$$

$$= G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot c_0$$

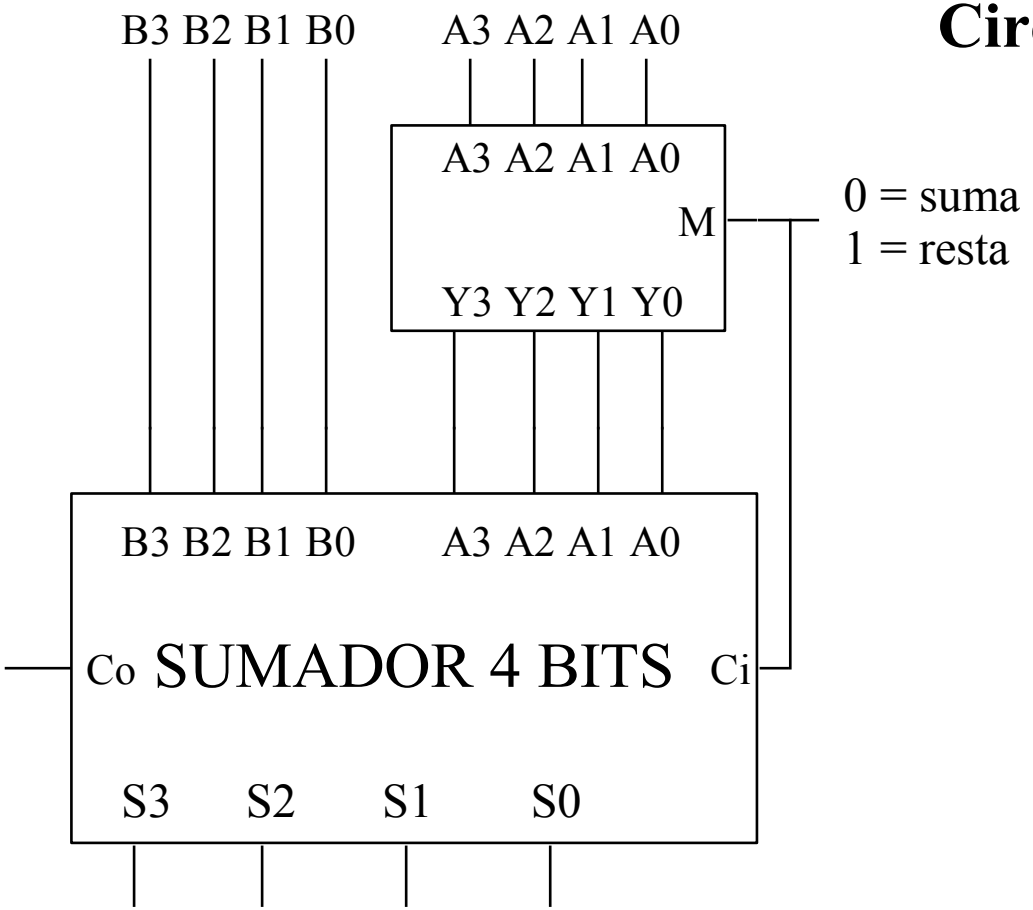
$$c_3 = G_2 + P_2 \cdot c_2$$

$$= G_2 + P_2 \cdot G_1 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot P_1 \cdot P_0 \cdot c_0$$



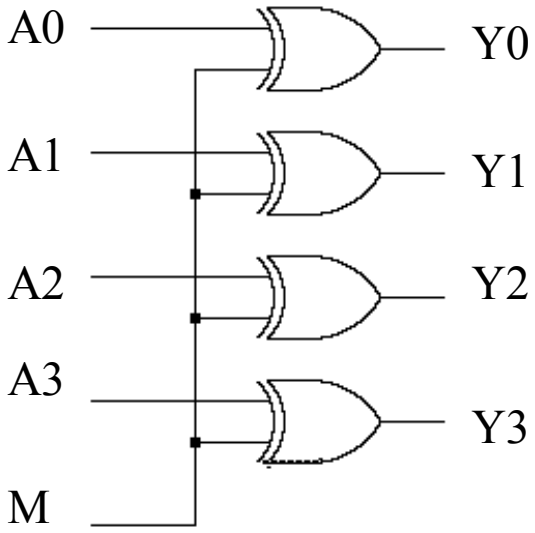
Pi y Gi sólo dependen de Ai y Bi y no de otras A y B => cálculo rápido

Sumador/Restador en complemento a 2



Circuito complementador a 1

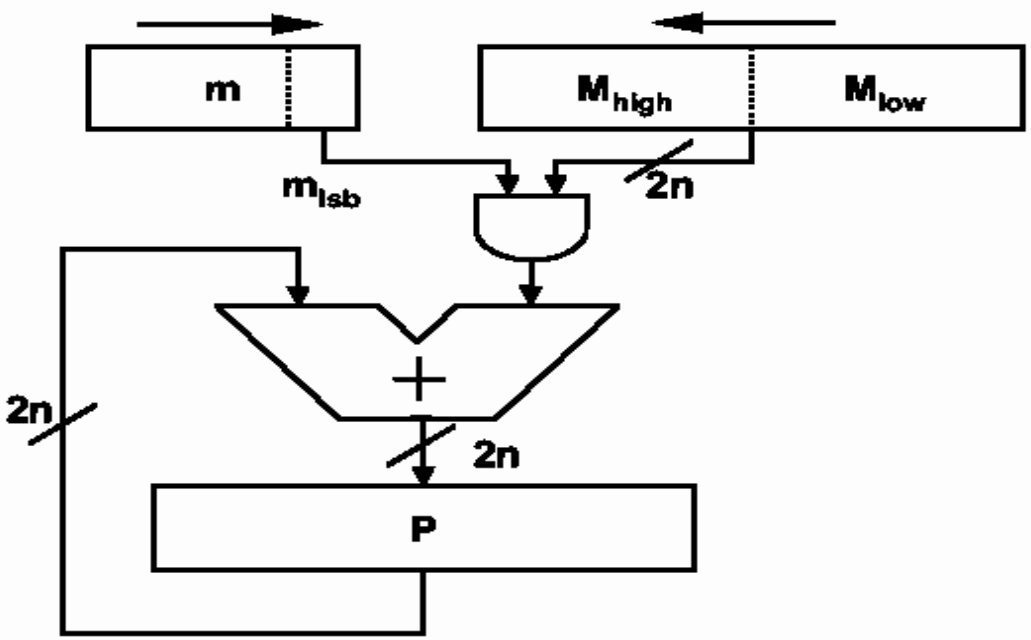
Ai	M	Yi
0	0	0
1	0	1
0	1	1
1	1	0



Multiplicadores

	1011	*multiplicando*
×	1101	*multiplicador*
	1011	
	0000	*productos parciales*
	1011	
+	1011	
	10001111	*producto*

multiplicación lenta
circuito de control complejo

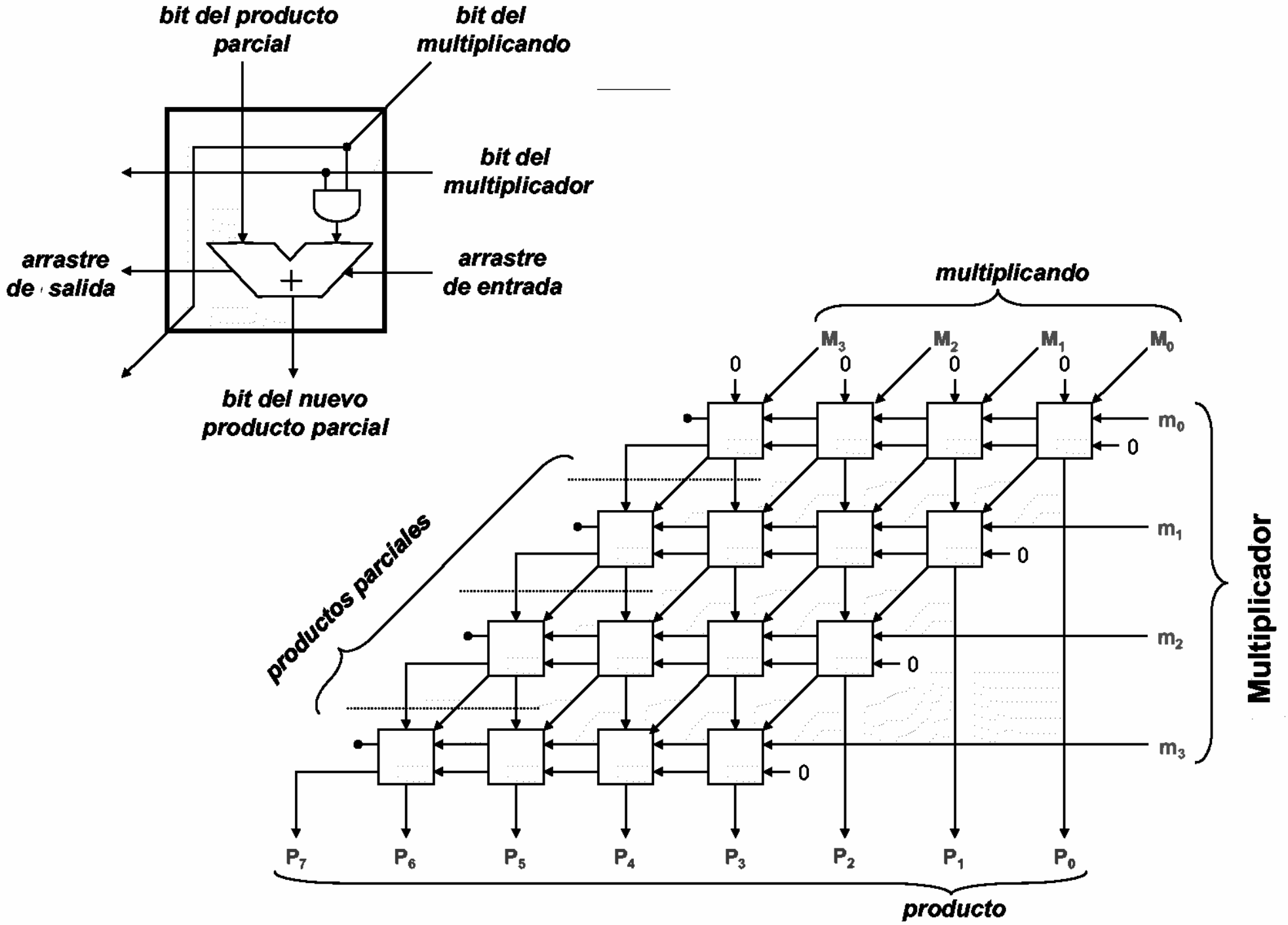


S0 : cargar multiplicador en *m*
cargar multiplicando en M_{low}
borrar M_{high}
borrar *P*

S1 : si m_{lsb} = 1 entonces $P \leftarrow P+M$
si m_{lsb} = 0 entonces $P \leftarrow P+0$

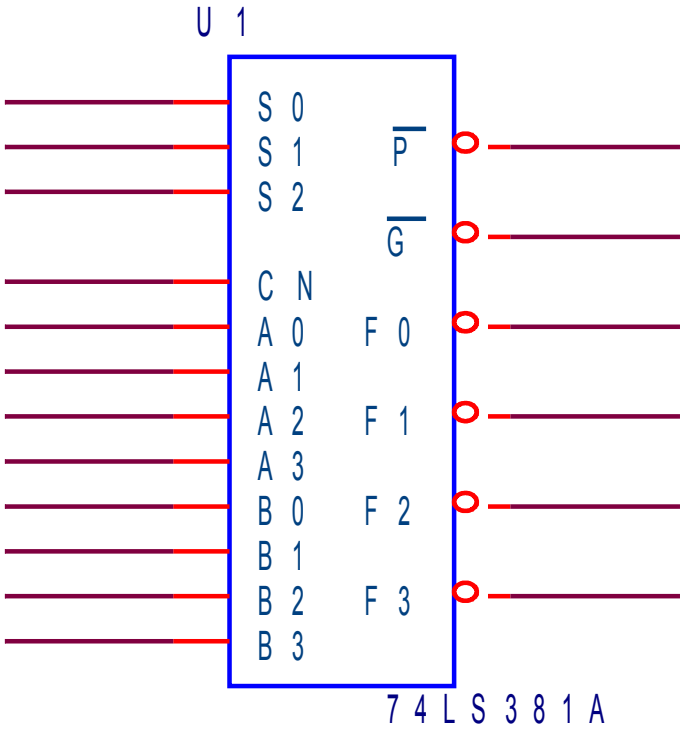
S2 : desplazar *M* a la izquierda
desplazar *m* a la derecha
si *S1*-*S2* no se han repetido *n* veces, ir a *S1*

Multiplicador rápido (combinacional)



Unidad Aritmético-Lógica

SELECCIÓN	OPERACIÓN ARITMÉTICO/ LÓGICA
S2 S1 S0	
0 0 0	CLEAR
0 0 1	B menos A
0 1 0	A menos B
0 1 1	A mas B
1 0 0	A XOR B
1 0 1	A + B
1 1 0	A * B
1 1 1	PRESET



- Las operaciones XOR, + y - son lógicas son bit a bit
- Las operaciones mas y menos son aritméticas
- La tabla de verdad (hoja siguiente) es una versión reducida, donde están sólo algunas combinaciones

FUNCTION TABLE

ARITHMETIC/LOGIC OPERATION	INPUTS						OUTPUTS				('LS381A, 'S381)		('LS382A)	
	S2	S1	S0	C_n	A_n	B_n	F3	F2	F1	F0	$\overline{G}$	$\overline{P}$	OVR	C_{n+4}
CLEAR	L	L	L	X	X	X	L	L	L	L	H	H	L	L
B MINUS A	L	L	H	L	L	L	H	H	H	H	H	L	L	L
				L	L	H	H	H	H	L	L	H	L	H
				L	H	L	L	L	L	L	H	H	L	L
				L	H	H	H	H	H	H	H	L	L	L
				H	L	L	L	L	L	L	H	L	L	H
				H	L	H	H	H	H	H	L	H	L	H
				H	H	L	L	L	L	H	H	H	L	L
				H	H	H	L	L	L	L	H	H	L	H
A MINUS B	L	H	L	L	L	L	H	H	H	H	H	L	L	L
				L	L	H	L	L	L	L	H	H	L	L
				L	H	L	H	H	H	L	L	H	L	H
				L	H	H	H	H	H	H	H	L	L	L
				H	L	L	L	L	L	L	H	L	L	H
				H	L	H	L	L	L	H	H	H	L	L
				H	H	L	H	H	H	H	L	H	L	H
				H	H	H	L	L	L	L	H	H	L	H
A PLUS B	L	H	H	L	L	L	L	L	L	L	H	H	L	L
				L	L	H	H	H	H	H	H	L	L	L
				L	H	L	H	H	H	H	H	L	L	L
				L	H	H	H	H	H	L	L	H	L	H
				H	L	L	L	L	L	H	H	H	L	L
				H	L	H	L	L	L	L	H	L	L	H
				H	H	L	L	L	L	L	H	L	L	H
				H	H	H	H	H	H	H	L	H	L	H
A ⊕ B	H	L	L	X	L	L	L	L	L	L	H	H	L	L
				L	L	H	H	H	H	H	H	L	L	L
				H	L	H	H	H	H	H	H	L	H	H
				L	H	L	H	H	H	H	H	L	L	L
				H	H	L	H	H	H	H	H	L	H	H
				X	H	H	L	L	L	L	H	H	L	L
A + B	H	L	H	X	L	L	L	L	L	L	H	H	L	L
				L	L	H	H	H	H	H	H	L	L	L
				H	L	H	H	H	H	H	H	L	H	H
				L	H	L	H	H	H	H	H	L	L	L
				H	H	L	H	H	H	H	H	L	H	H
				L	H	H	H	H	H	H	H	L	L	L
				H	H	H	H	H	H	H	H	L	H	H
AB	H	H	L	X	L	L	L	L	L	L	H	H	L	L
				X	L	H	L	L	L	L	H	H	L	L
				X	H	L	L	L	L	L	H	H	L	L
				L	H	H	H	H	H	H	H	L	L	L
				H	H	H	H	H	H	H	H	L	H	H
PRESET	H	H	H	L	X	X	H	H	H	H	H	L	L	L
				H	X	X	H	H	H	H	H	L	H	H