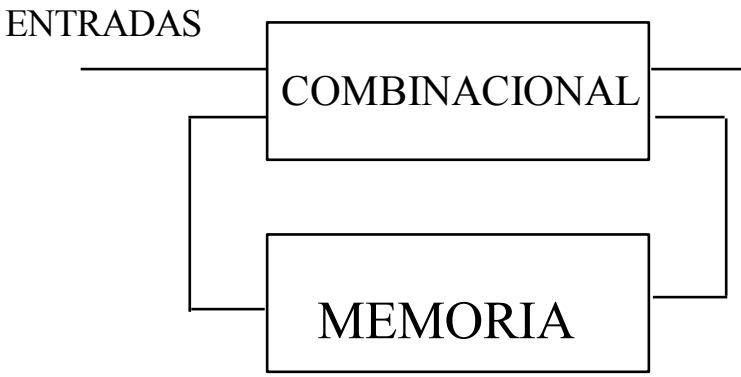
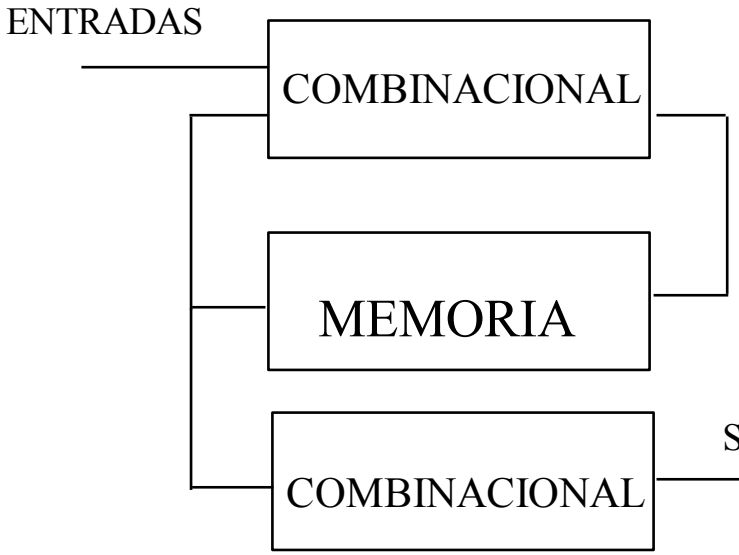
Circuitos secuenciales



MEALY

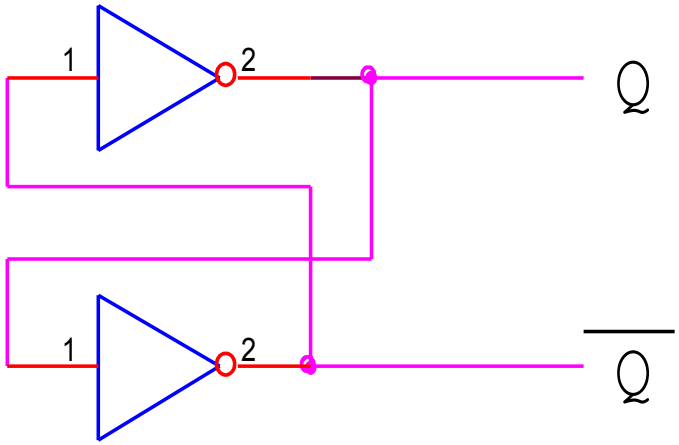


MOORE

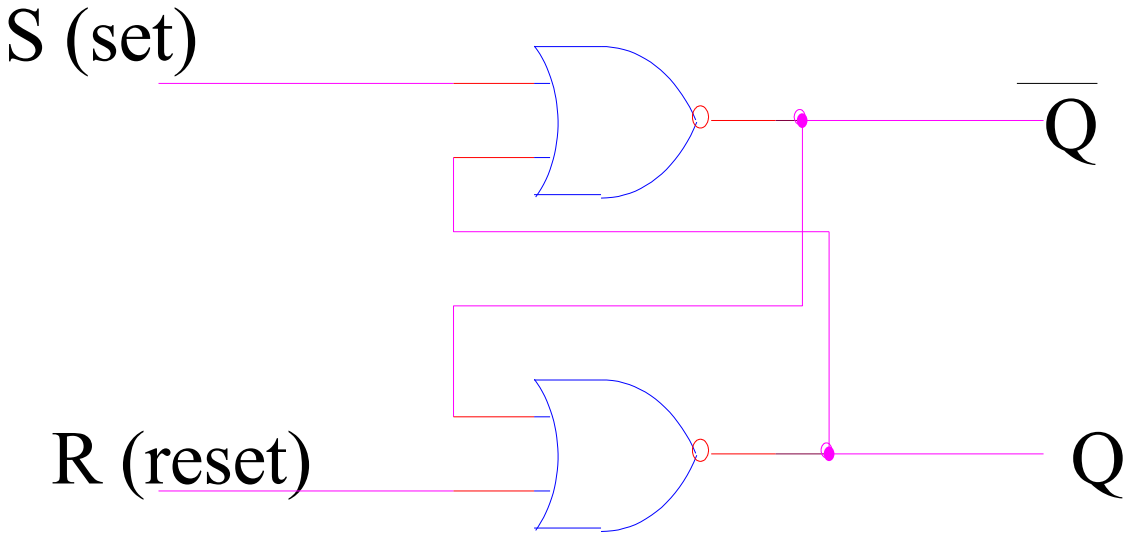
CLASIFICACIÓN

- Según la estructura
  - » Moore
  - » Mealy
- Según la evolución
  - » Síncronos
    - Por nivel
    - Por flanco
  - » Asíncronos

Elemento de memoria con dos inversores

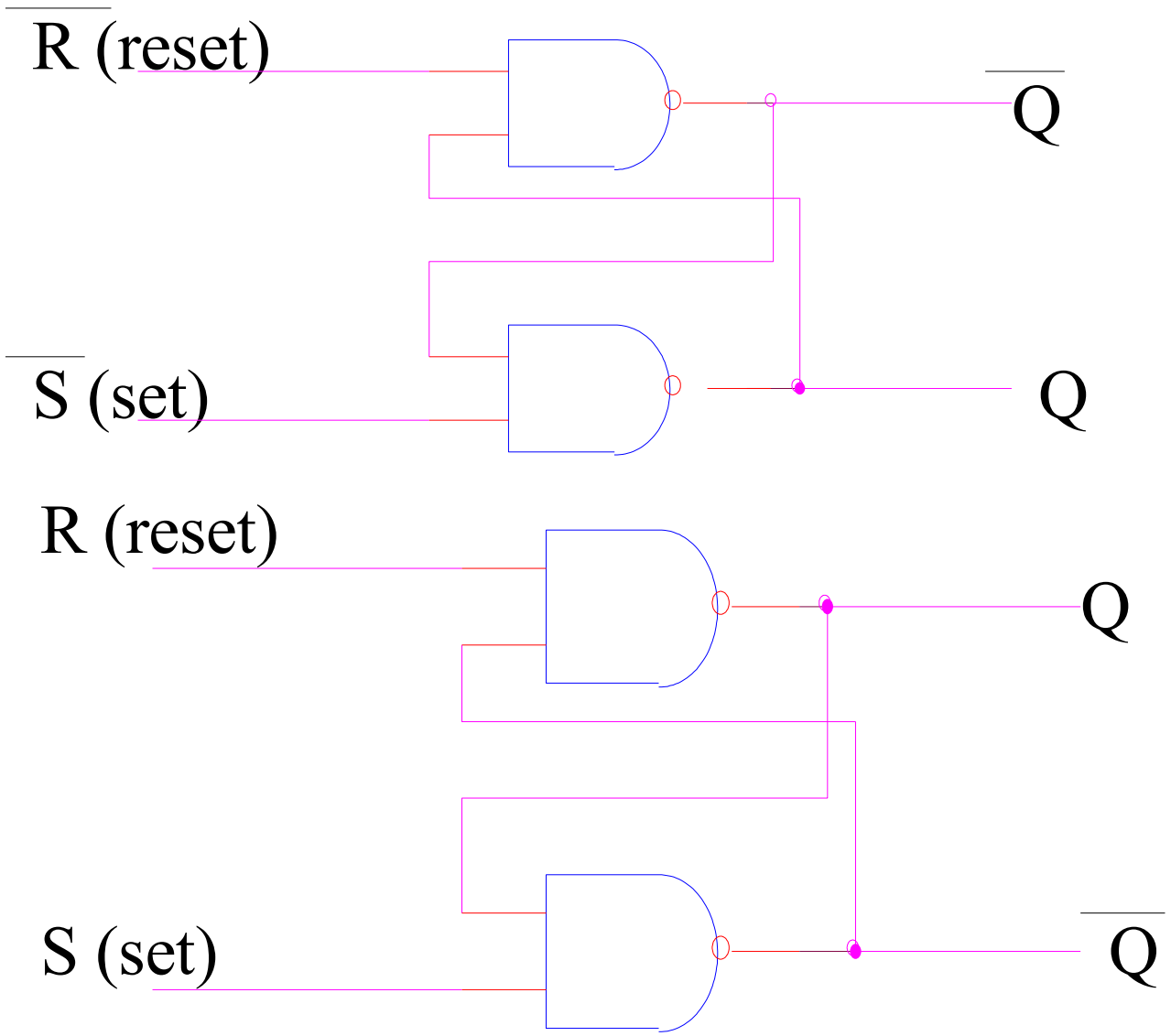


Biestable SR con puertas NOR

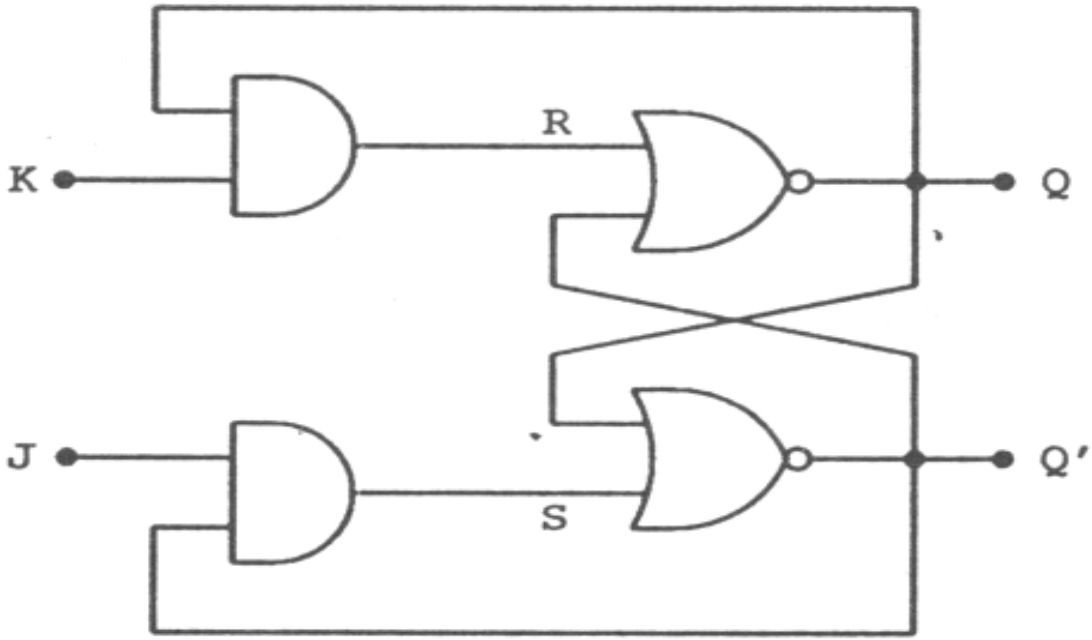


S	R	Q (t+1)
0	0	No cambia
0	1	0
1	0	1
1	1	No usada

Biestables RS



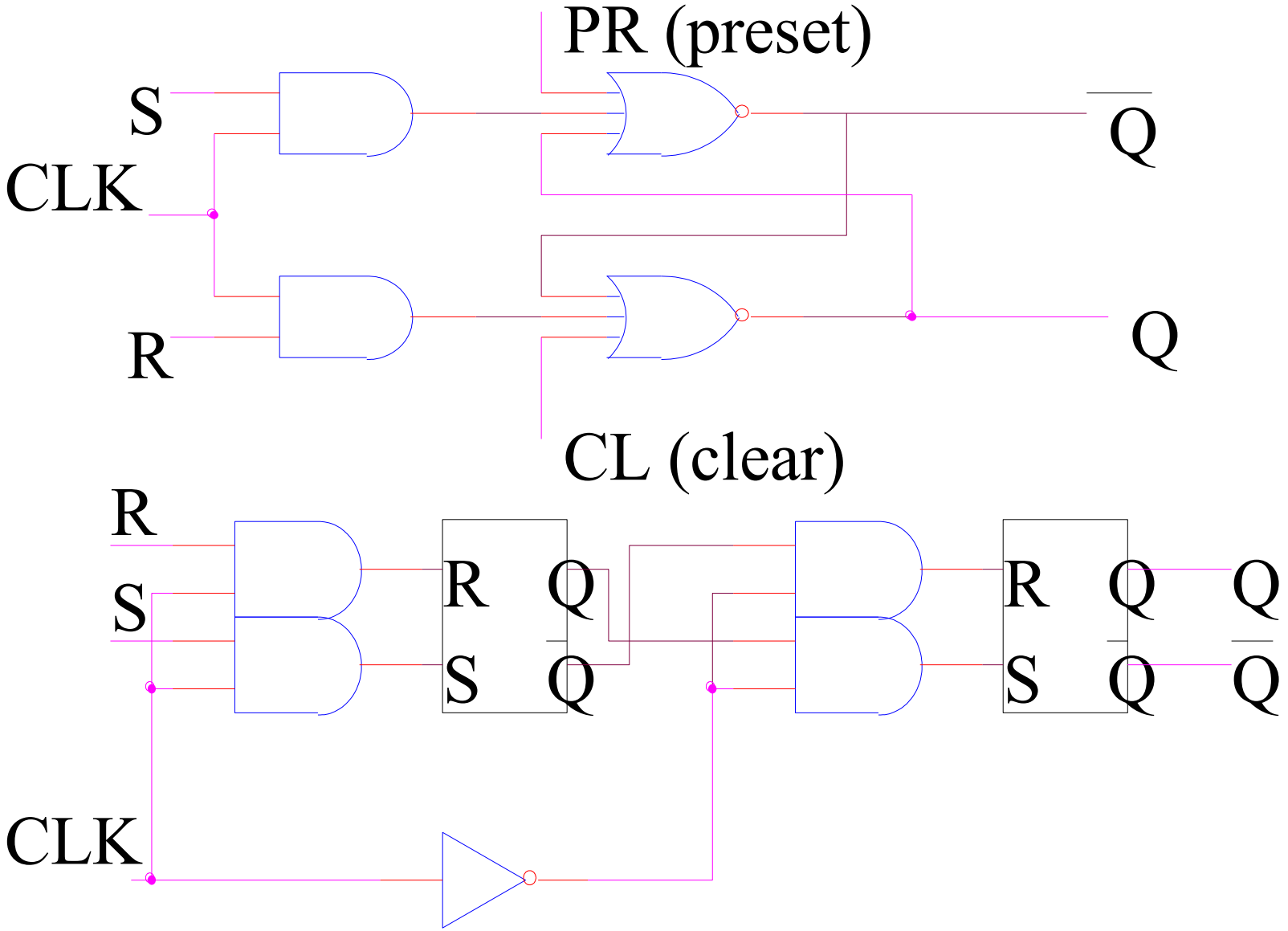
Biestable JK



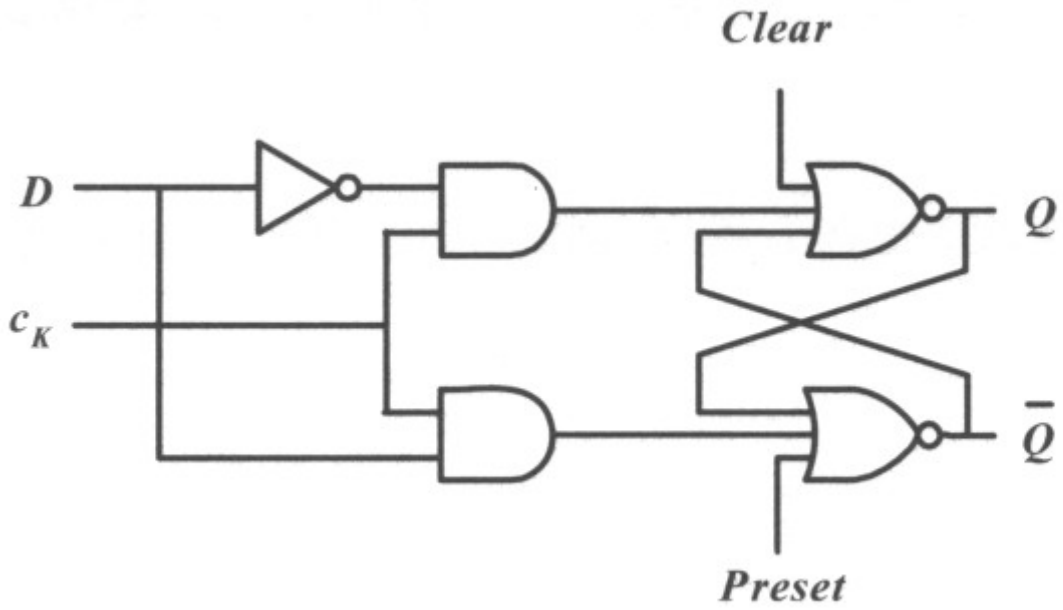
J K	Q_{t+1}	
0 0	Q_t	Estado anterior
0 1	0	Puesta a cero
1 0	1	Puesta a uno
1 1	$\overline{Q}_t$	Basculamiento

No válido sin sincronización -> sólo JK síncrono

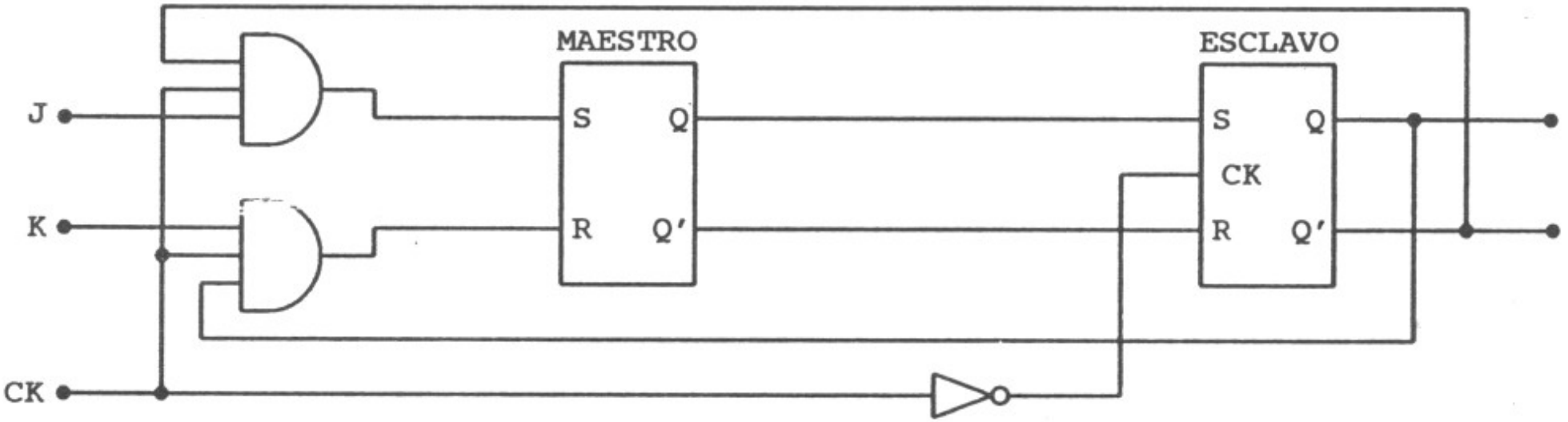
RS con PR y CL y flip-flop master-slave



Biestable D latch síncrono



Biestable JK síncrono maestro-esclavo



Flip-flop S-R disparado por flanco de subida

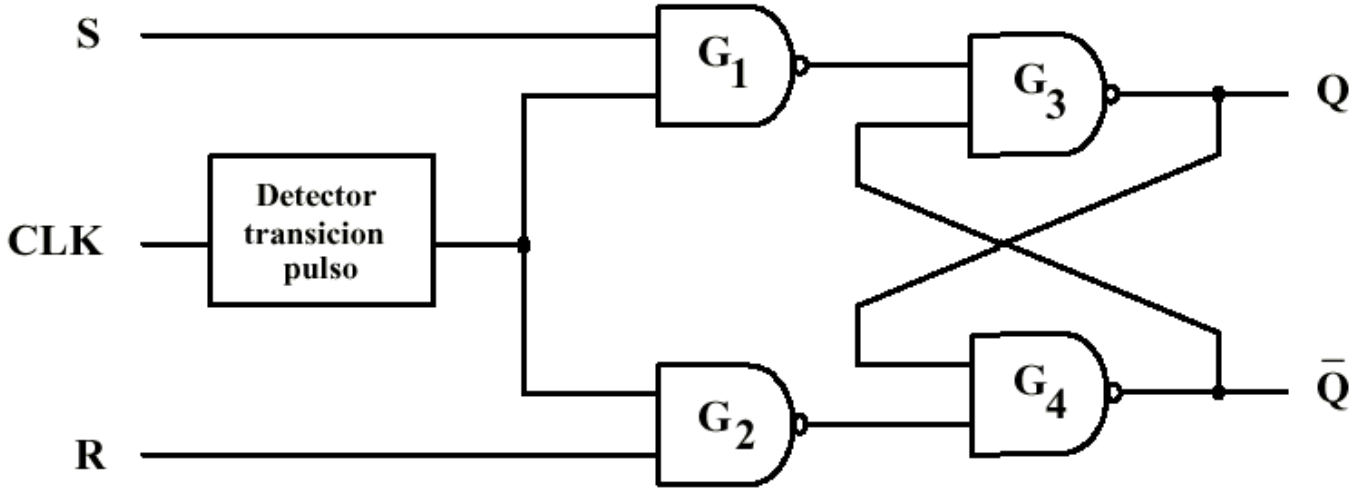


Tabla de verdad

Entradas			Salidas		Comentarios
S	R	CLK	Q	/Q	
0	0	X	Q_0	$/Q_0$	No cambia
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Condición no válida

Símbolo

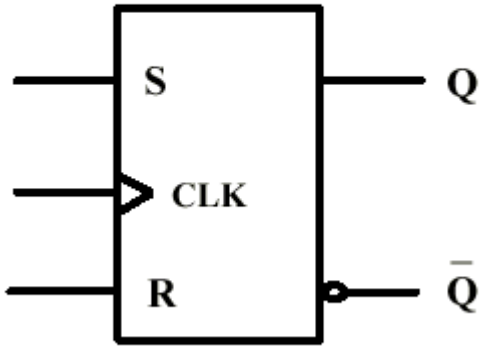
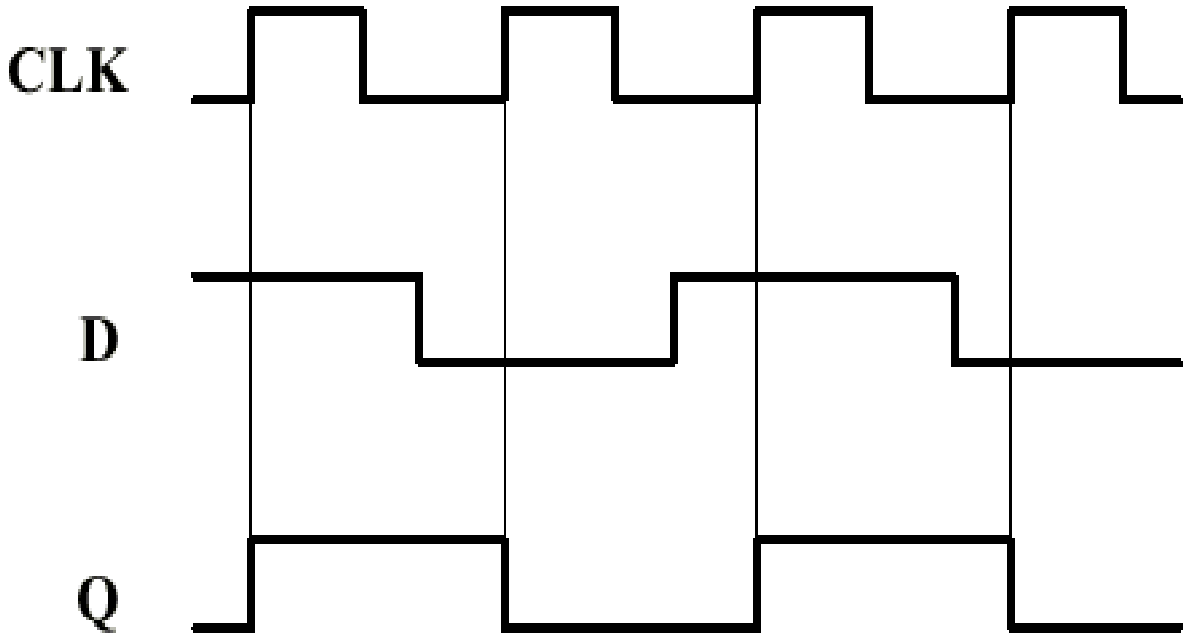


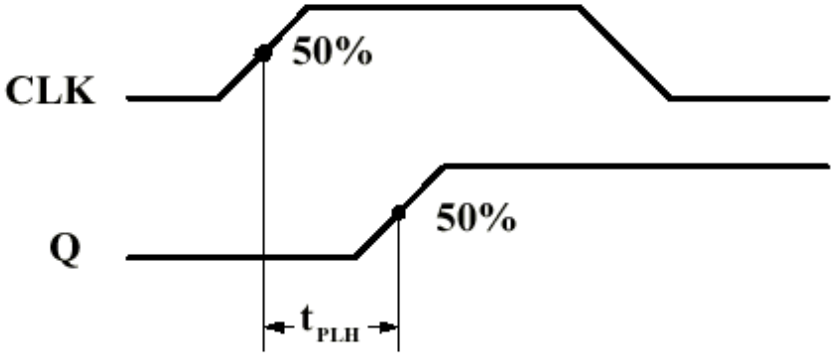
Tabla de verdad de un flip-flop D disparado por flanco de subida

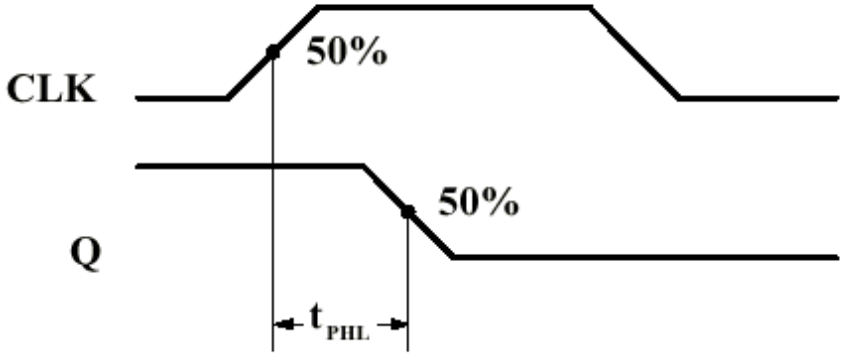
Entradas		Salidas		Comentarios
D	CLK	Q	/Q	
1	↑	1	0	SET
0	↑	0	1	RESET

Ejemplo

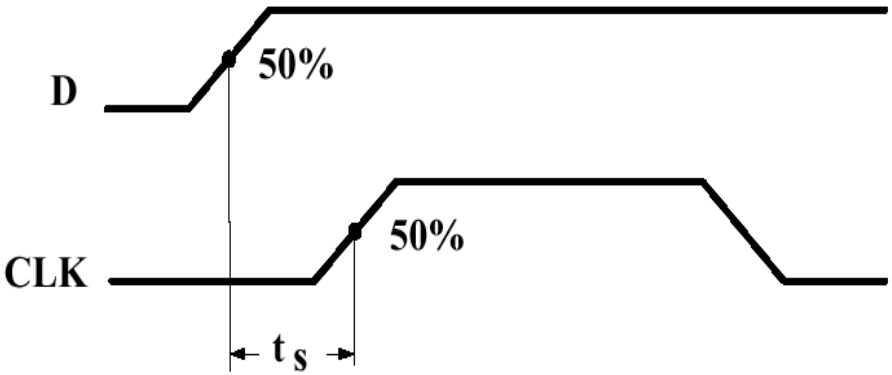


Tiempos de propagación

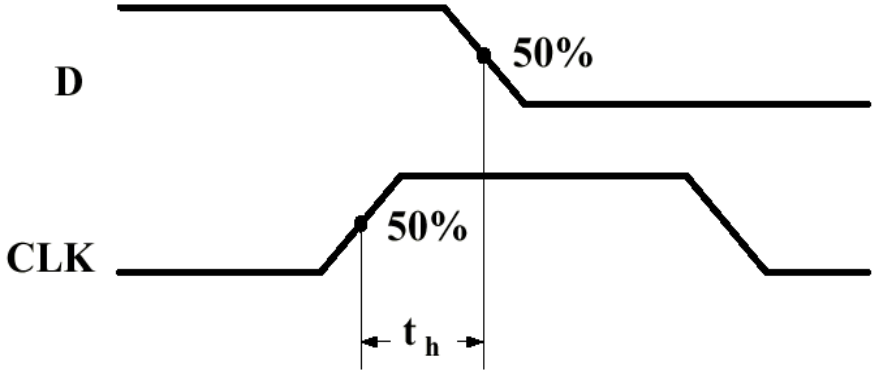




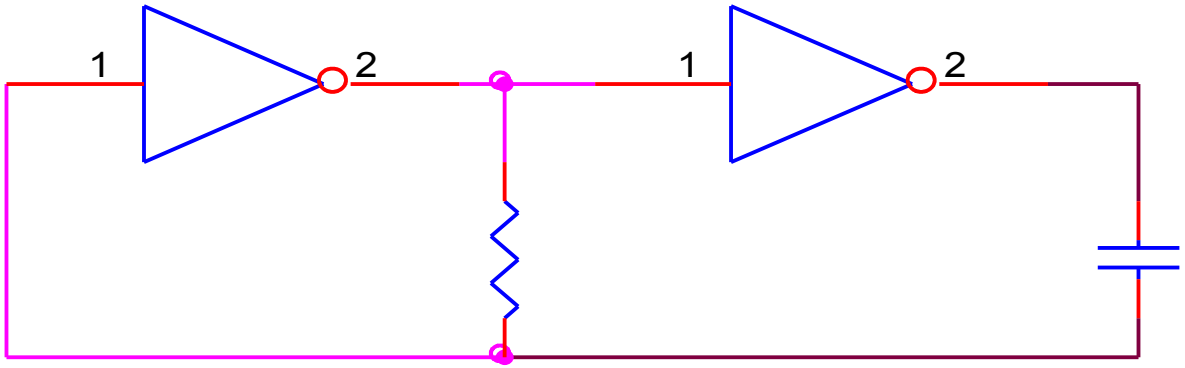
Tiempo de *set-up*

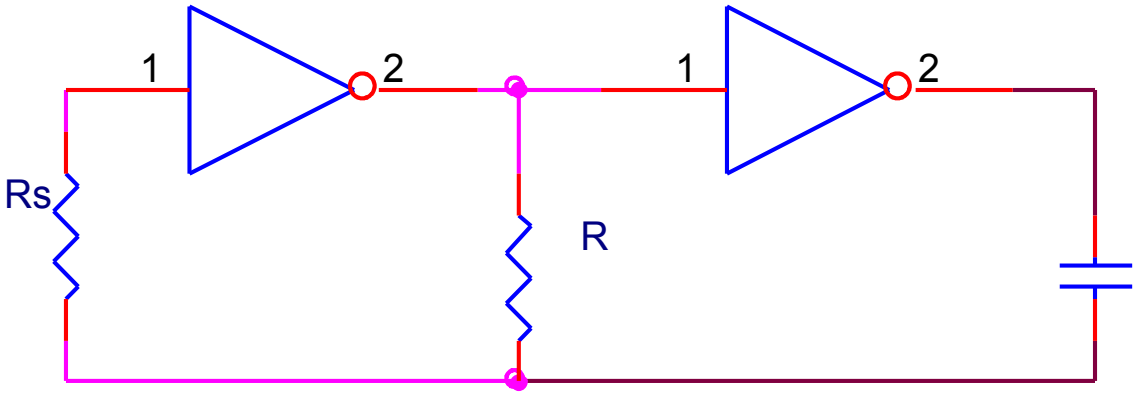


Tiempo de *hold*

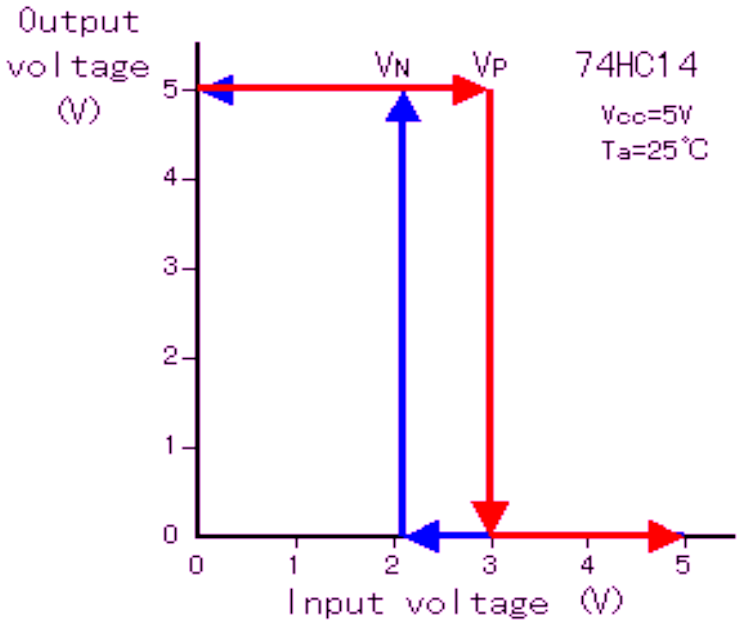


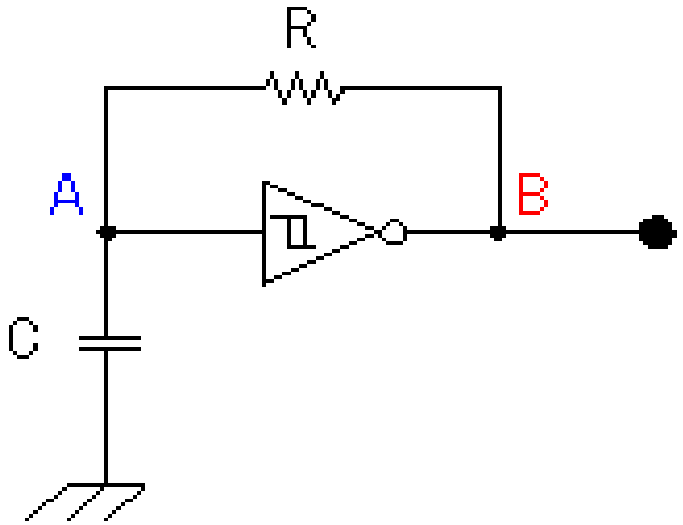
Aestables



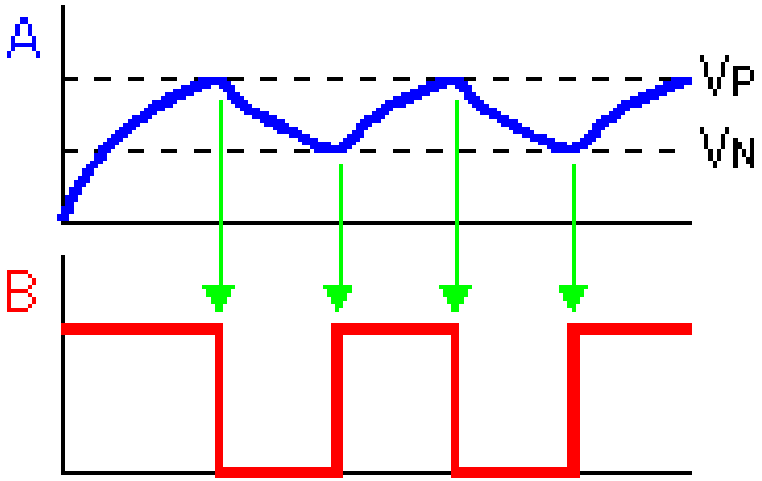


Aestable con negador trigger schmitt

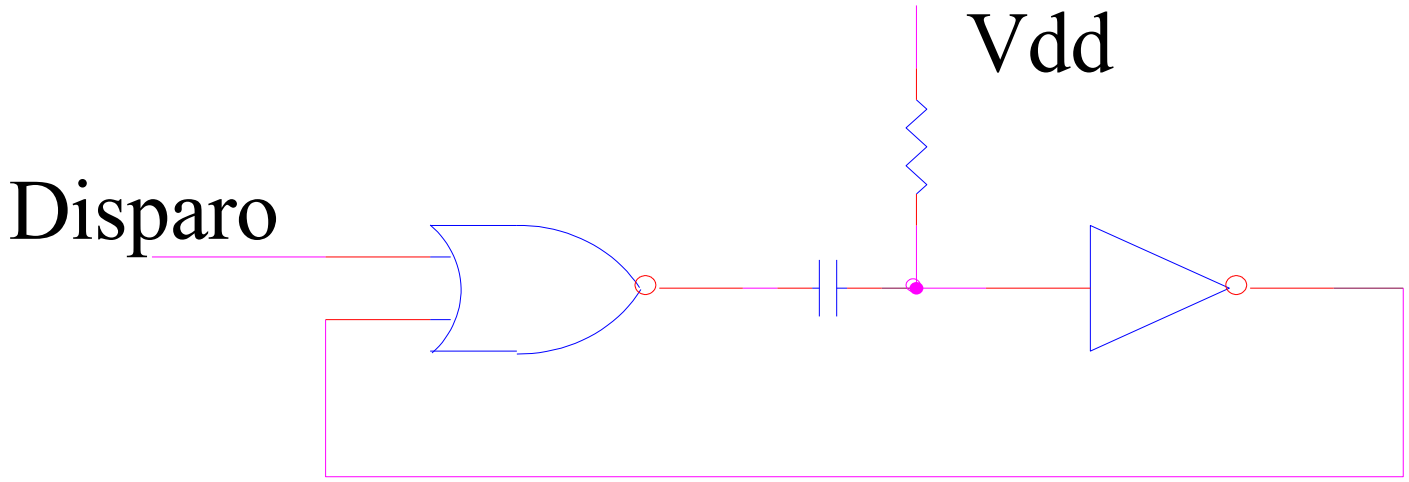


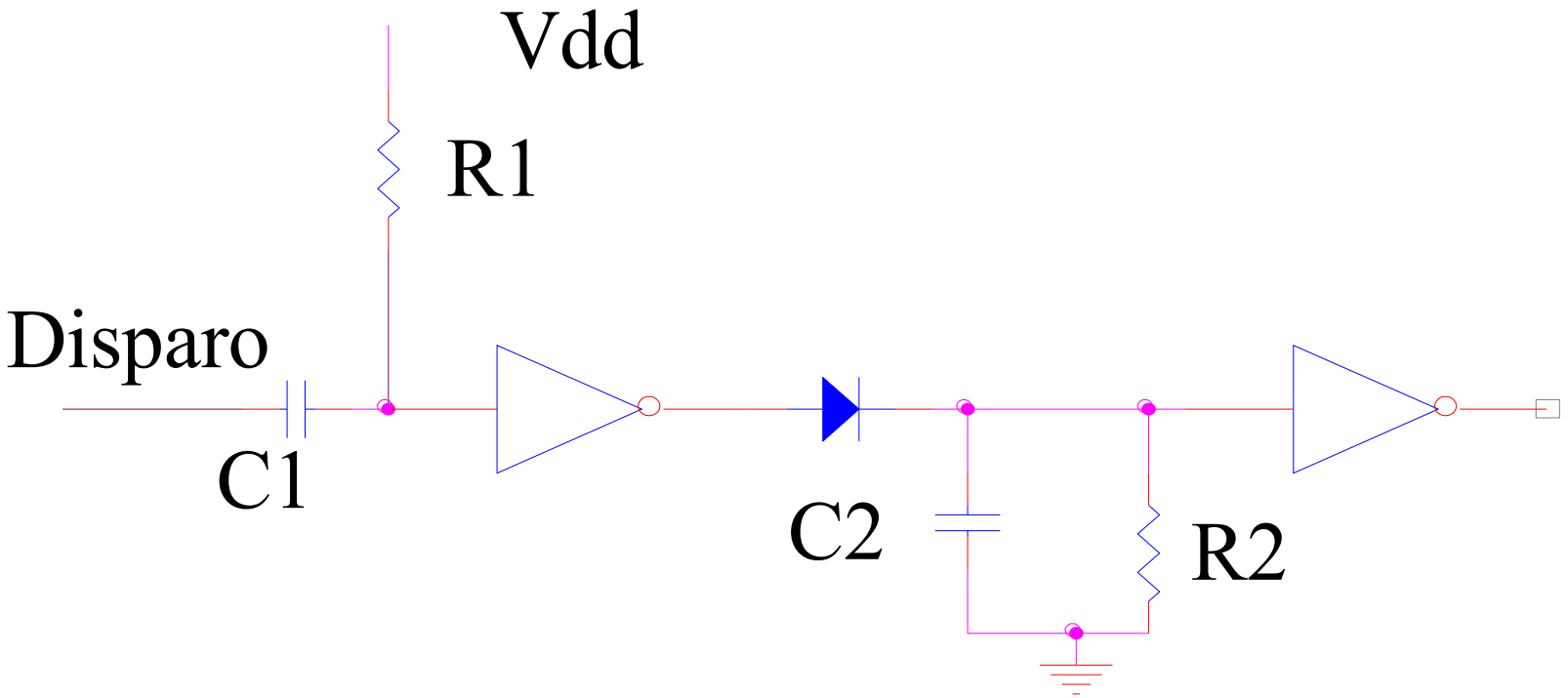


T=1'2 RC

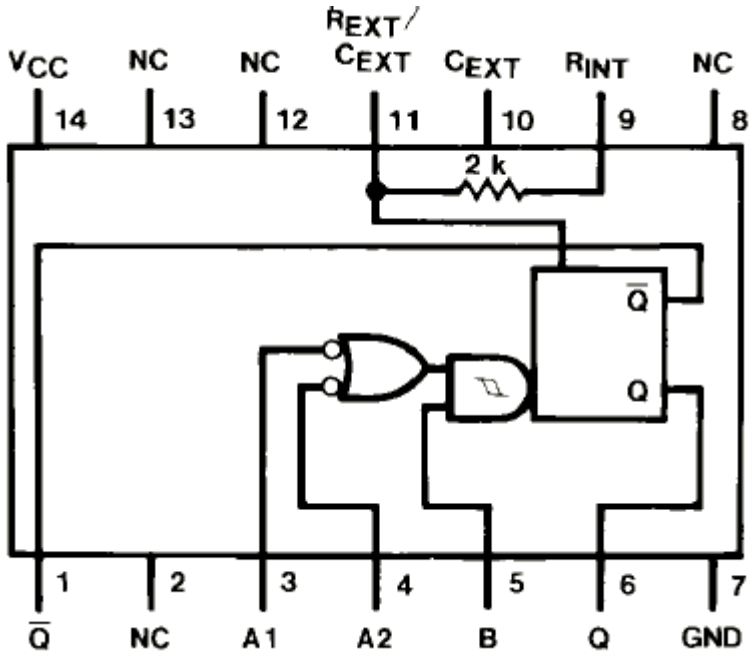


Monoestables





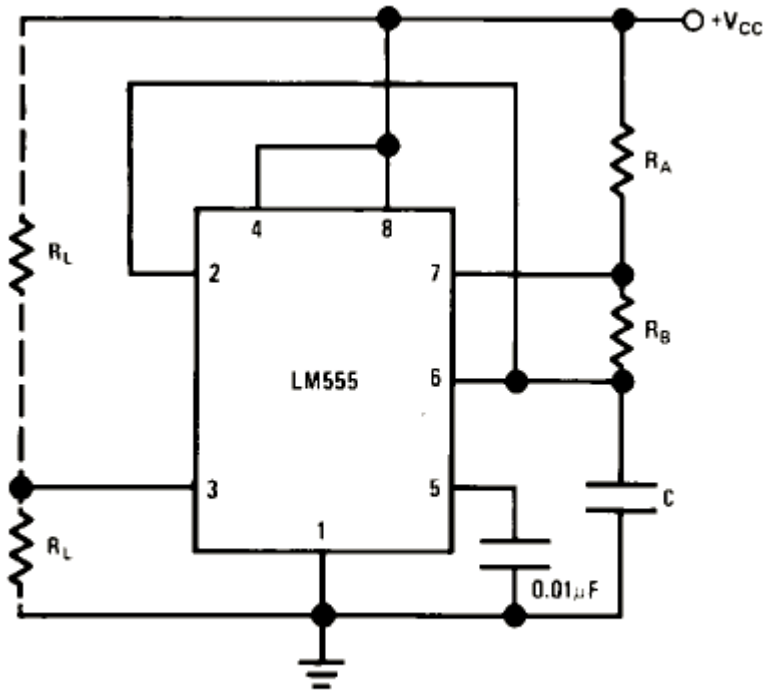
Monoestable con 74121



Function Table

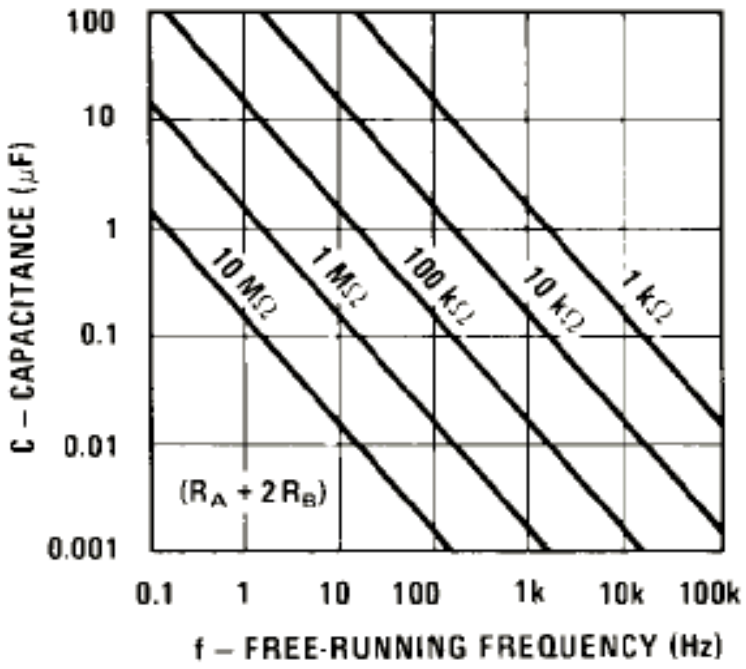
Inputs			Outputs	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎍
↓	H	H	⎍	⎍
↓	↓	H	⎍	⎍
L	X	↑	⎍	⎍
X	L	↑	⎍	⎍

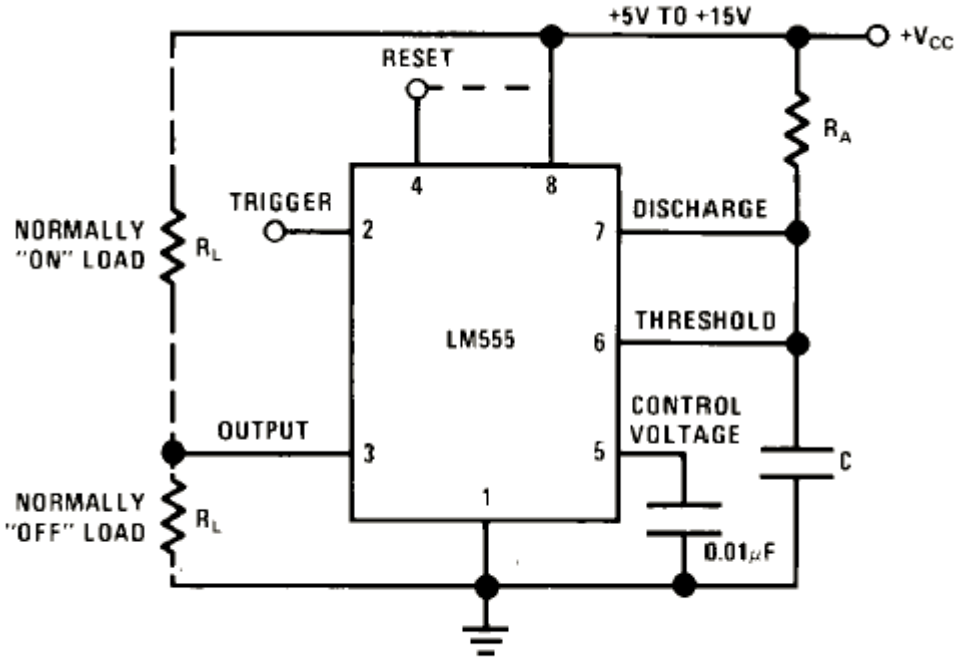
Aestables y monoestables con LM55



DS0078

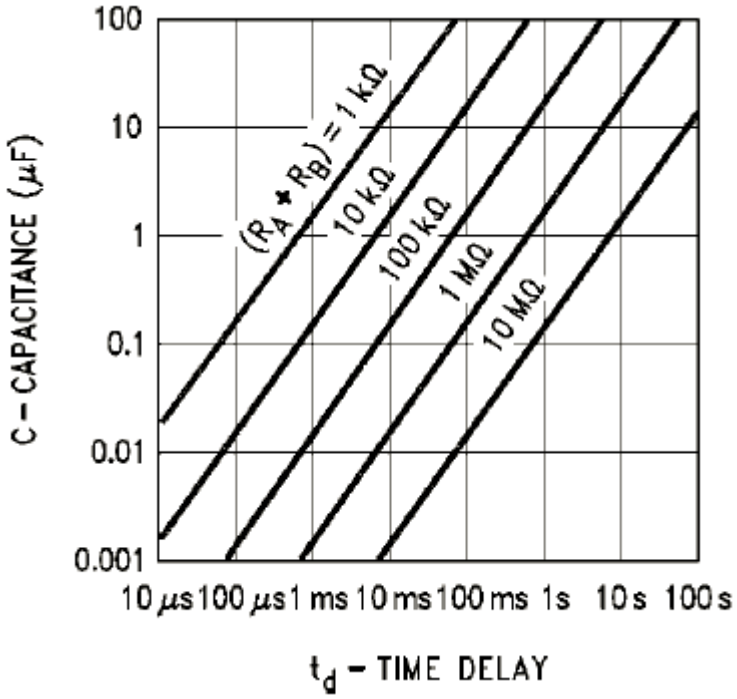
FIGURE 4. Astable





DS007851-5

FIGURE 1. Monostable



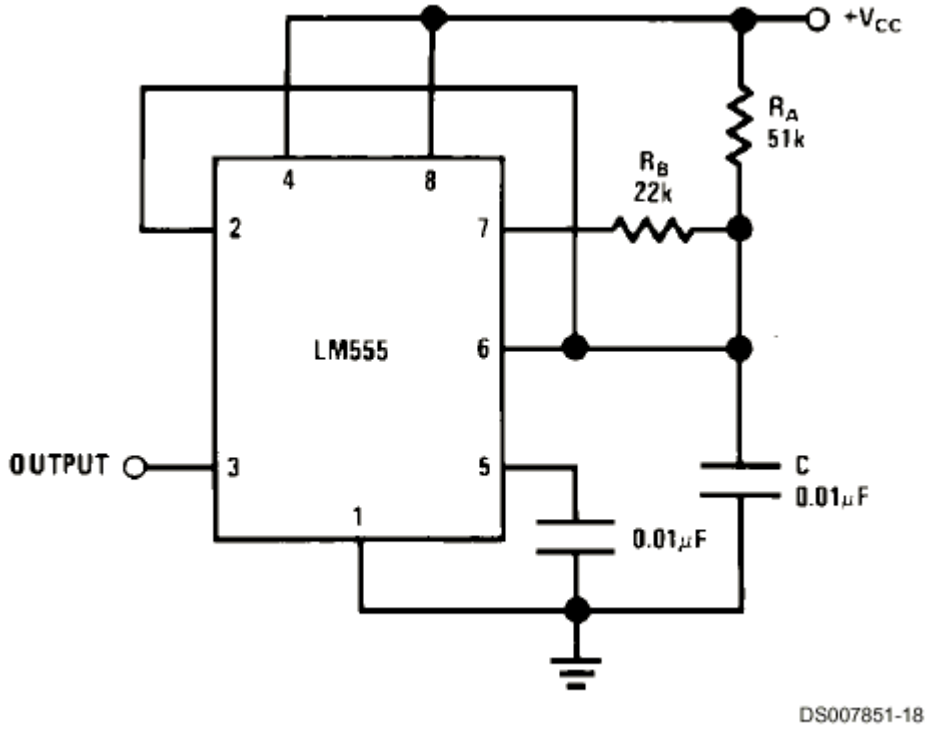


FIGURE 14. 50% Duty Cycle Oscillator