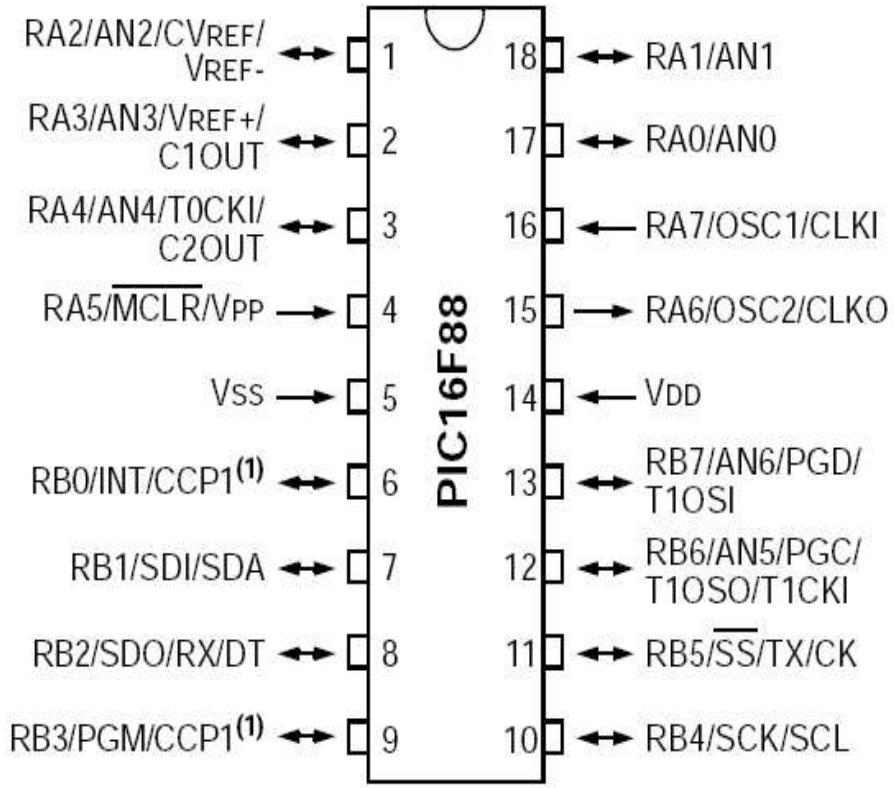
PIC16F88. Características

- Osciladores
  - Osciladores a cristal: LP, XT y HS hasta 20Mhz
  - Oscilador externo hasta 20Mhz
  - Oscilador interno: 31Khz – 8Mhz
- Periféricos
  - Módulo PWM/CCP
    - CCP (captura/comparación) -> 16 bits
    - PWM (modulación por pulsos) -> 10 bits
  - ADC 10bits 7 canales
  - SSP (puerto serie síncrono) -> SPI e I^2C
  - USART
  - Comparador analógico dual
- Características de bajo consumo (tecnología nanoWatt)

18-Pin PDIP, SOIC



Note 1: The CCP1 pin is determined by the CCPMX bit in Configuration Word 1 register.

Organización de la memoria

- 4K de memoria de programa (FLASH) organizada en 2 páginas (accesible mediante PCLATH)
- 4 bancos de memoria de datos (RAM) organizada en registros, accesibles mediante RP1/RP2 (status)

RP1:RP0	Bank
00	0
01	1
10	2
11	3

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK: PIC16F87/88

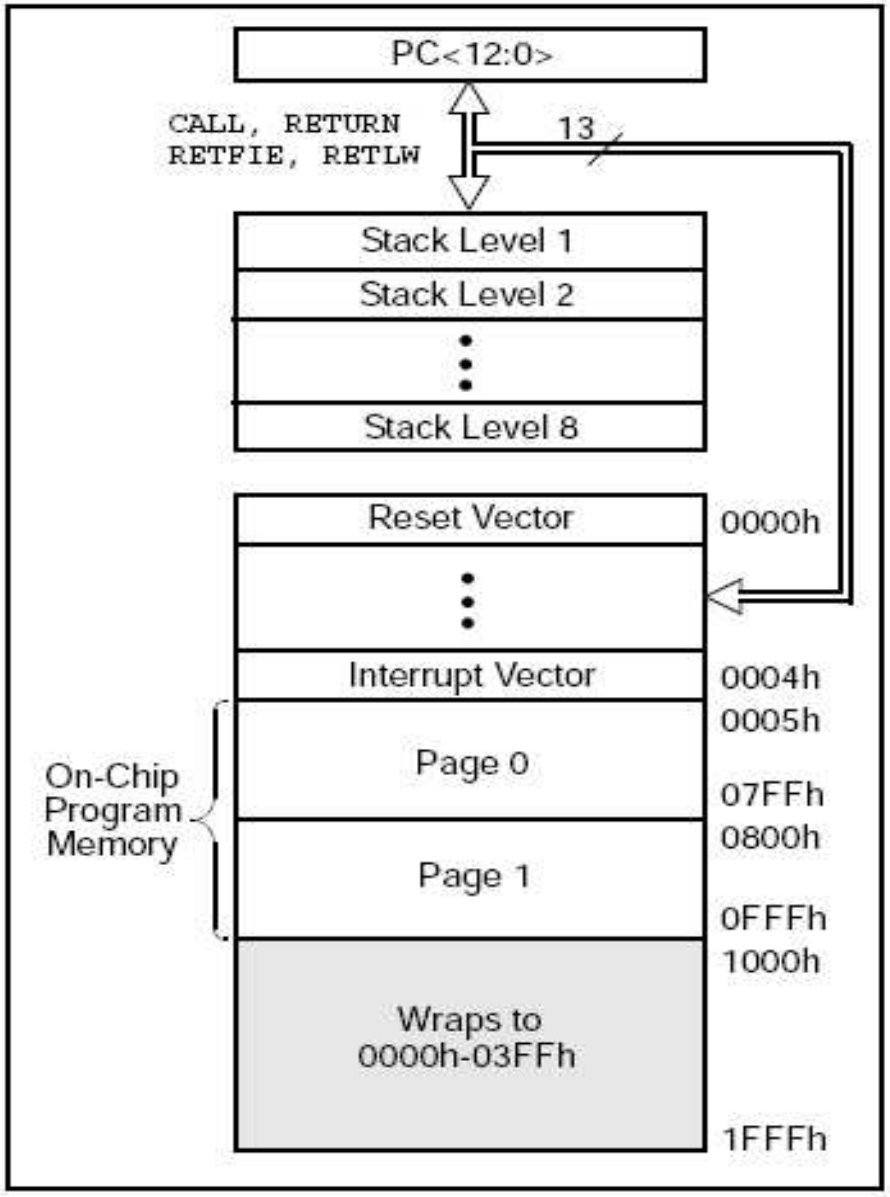
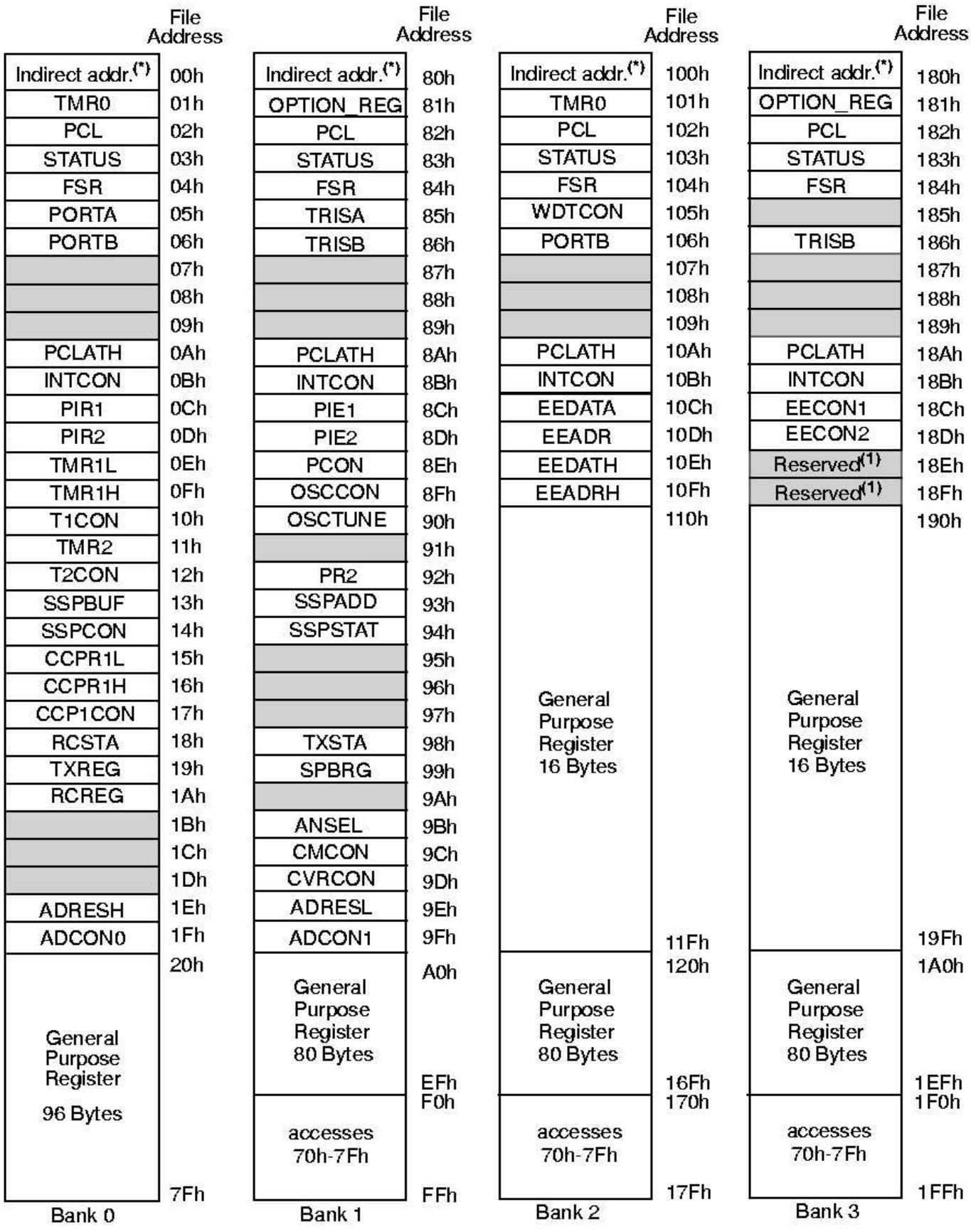


FIGURE 2-3: PIC16F88 REGISTER FILE MAP



Unimplemented data memory locations, read as '0'.

* Not a physical register.

Note 1: This register is reserved, maintain this register clear.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page
Bank 0											
00h(2)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	26, 135
01h	TMR0	Timer0 Module Register								xxxx xxxx	69
02h(2)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	
03h(2)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	17
04h(2)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	135
05h	PORTA	PORTA Data Latch when written; PORTA pins when read (PIC16F87) PORTA Data Latch when written; PORTA pins when read (PIC16F88)								xxxx 0000 xxx0 0000	52
06h	PORTB	PORTB Data Latch when written; PORTB pins when read (PIC16F87) PORTB Data Latch when written; PORTB pins when read (PIC16F88)								xxxx xxxx 00xx xxxx	58
07h	—	Unimplemented								—	—
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah(1,2)	PCLATH	—	—	—	Write Buffer for the Upper 5 bits of the Program Counter					---0 0000	135
0Bh(2)	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	19, 69, 77
0Ch	PIR1	—	ADIF(4)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	21, 77
0Dh	PIR2	OSFIF	CMIF	—	EEIF	—	—	—	—	00-0 ----	23, 34
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	77, 83
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	77, 83
10h	T1CON	—	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	-000 0000	72, 83
11h	TMR2	Timer2 Module Register								0000 0000	80, 85
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	80, 85
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	90, 95
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	89, 95
15h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxx	83, 85
16h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxx	83, 85
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	81, 83
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	98, 99
19h	TXREG	AUSART Transmit Data Register								0000 0000	103
1Ah	RCREG	AUSART Receive Data Register								0000 0000	105
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	ADRESH(4)	A/D Result Register High Byte								xxxx xxxx	120
1Fh	ADCON0(4)	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	—	ADON	0000 00-0	114, 120

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for PC<12:8>, whose contents are transferred to the upper byte of the program counter.

2: These registers can be addressed from any bank.

3: RA5 is an input only; the state of the TRISA5 bit has no effect and will always read '1'.

4: PIC16F88 device only.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page
Bank 1											
80h(2)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	26, 135
81h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	16, 69
82h(2)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	135
83h(2)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	17
84h(2)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	135
85h	TRISA	TRISA7	TRISA6	TRISA5(3)	PORTA Data Direction Register (TRISA<4:0>)					1111 1111	52, 126
86h	TRISB	PORTB Data Direction Register								1111 1111	58, 85
87h	—	Unimplemented								—	—
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah(1,2)	PCLATH	—	—	—	Write Buffer for the Upper 5 bits of the Program Counter					---0 0000	135
8Bh(2)	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	19, 69, 77
8Ch	PIE1	—	ADIE(4)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	20, 80
8Dh	PIE2	OSFIE	CMIE	—	EEIE	—	—	—	—	00-0 ----	22, 84
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$	---- --0q	24
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	IOFS	SCS1	SCS0	-000 0000	40
90h	OSCTUNE	—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0	--00 0000	38
91h	—	Unimplemented								—	—
92h	PR2	Timer2 Period Register								1111 1111	80, 85
93h	SSPADD	Synchronous Serial Port (I^2C™ mode) Address Register								0000 0000	95
94h	SSPSTAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000 0000	88, 95
95h	—	Unimplemented								—	—
96h	—	Unimplemented								—	—
97h	—	Unimplemented								—	—
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	97, 99
99h	SPBRG	Baud Rate Generator Register								0000 0000	99, 103
9Ah	—	Unimplemented								—	—
9Bh	ANSEL(4)	—	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	-111 1111	120
9Ch	CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0111	121, 126, 126
9Dh	CVRCON	CVREN	CVROE	CVRR	—	CVR3	CVR2	CVR1	CVR0	000- 0000	126, 126
9Eh	ADRESL(4)	A/D Result Register Low Byte								xxxx xxxx	120
9Fh	ADCON1(4)	ADFM	ADCS2	VCFG1	VCFG0	—	—	—	—	0000 ----	52, 115, 120

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for PC<12:8>, whose contents are transferred to the upper byte of the program counter.

2: These registers can be addressed from any bank.

3: RA5 is an input only; the state of the TRISA5 bit has no effect and will always read '1'.

4: PIC16F88 device only.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page
Bank 2											
100h(2)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	26, 135
101h	TMR0	Timer0 Module Register								xxxx xxxx	69
102h(2)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	135
103h(2)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	17
104h(2)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	135
105h	WDTCON	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	---0 1000	142
106h	PORTB	PORTB Data Latch when written; PORTB pins when read (PIC16F87) PORTB Data Latch when written; PORTB pins when read (PIC16F88)								xxxx xxxx 00xx xxxx	58
107h	—	Unimplemented								—	—
108h	—	Unimplemented								—	—
109h	—	Unimplemented								—	—
10Ah(1,2)	PCLATH	—	—	—	Write Buffer for the Upper 5 bits of the Program Counter					---0 0000	135
10Bh(2)	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	19, 69, 77
10Ch	EEDATA	EEPROM/Flash Data Register Low Byte								xxxx xxxx	34
10Dh	EEADR	EEPROM/Flash Address Register Low Byte								xxxx xxxx	34
10Eh	EEDATH	—	—	EEPROM/Flash Data Register High Byte						--xx xxxx	34
10Fh	EEADRH	—	—	—	—	EEPROM/Flash Address Register High Byte				---- xxxx	34
Bank 3											
180h(2)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	135
181h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	18, 69
182h(2)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	135
183h(2)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	17
184h(2)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	135
185h	—	Unimplemented								—	—
186h	TRISB	PORTB Data Direction Register								1111 1111	58, 83
187h	—	Unimplemented								—	—
188h	—	Unimplemented								—	—
189h	—	Unimplemented								—	—
18Ah(1,2)	PCLATH	—	—	—	Write Buffer for the Upper 5 bits of the Program Counter					---0 0000	135
18Bh(2)	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	19, 69, 77
18Ch	EECON1	EEPGD	—	—	FREE	WRERR	WREN	WR	RD	x---x x000	26, 34
18Dh	EECON2	EEPROM Control Register 2 (not a physical register)								---- ----	34
18Eh	—	Reserved, maintain clear								0000 0000	—
18Fh	—	Reserved, maintain clear								0000 0000	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for PC<12:8>, whose contents are transferred to the upper byte of the program counter.

2: These registers can be addressed from any bank.

3: RA5 is an input only; the state of the TRISA5 bit has no effect and will always read '1'.

4: PIC16F88 device only.

Registros de control iguales que PIC16F84

REGISTER 2-1: STATUS: ARITHMETIC STATUS REGISTER (ADDRESS 03h, 83h, 103h, 183h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7							bit 0

bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)
1 = Bank 2, 3 (100h-1FFh)
0 = Bank 0, 1 (00h-FFh)

bit 6-5 **RP<1:0>:** Register Bank Select bits (used for direct addressing)
11 = Bank 3 (180h-1FFh)
10 = Bank 2 (100h-17Fh)
01 = Bank 1 (80h-FFh)
00 = Bank 0 (00h-7Fh)
Each bank is 128 bytes.

bit 4 **$\overline{TO}$:** Time-out bit
1 = After power-up, CLRWDT instruction or SLEEP instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-Down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit carry/$\overline{borrow}$ bit (ADDWF, ADDLW, SUBLW and SUBWF instructions)(1)
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{borrow}$ bit (ADDWF, ADDLW, SUBLW and SUBWF instructions)(1,2)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand.

2: For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low-order bit of the source register.

REGISTER 2-2: OPTION_REG: OPTION CONTROL REGISTER (ADDRESS 81h, 181h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7 **$\overline{\text{RBPU}}$**: PORTB Pull-up Enable bit

1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

bit 6 **INTEDG:** Interrupt Edge Select bit

1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5 **T0CS:** TMR0 Clock Source Select bit

1 = Transition on RA4/T0CKI/C2OUT pin
0 = Internal instruction cycle clock (CLKO)

bit 4 **T0SE:** TMR0 Source Edge Select bit

1 = Increment on high-to-low transition on RA4/T0CKI/C2OUT pin
0 = Increment on low-to-high transition on RA4/T0CKI/C2OUT pin

bit 3 **PSA:** Prescaler Assignment bit

1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

REGISTER 2-3: INTCON: INTERRUPT CONTROL REGISTER (ADDRESS 0Bh, 8Bh, 10Bh, 18Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
bit 7							bit 0

bit 7 **GIE:** Global Interrupt Enable bit

1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit

1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **TMR0IE:** TMR0 Overflow Interrupt Enable bit

1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4 **INT0IE:** RB0/INT External Interrupt Enable bit

1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3 **RBIE:** RB Port Change Interrupt Enable bit

1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2 **TMR0IF:** TMR0 Overflow Interrupt Flag bit

1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INT0IF:** RB0/INT External Interrupt Flag bit

1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0 **RBIF:** RB Port Change Interrupt Flag bit

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

Registros de control distintos que PIC16F84

REGISTER 2-4: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1 (ADDRESS 8Ch)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	ADIE(1)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6 **ADIE:** A/D Converter Interrupt Enable bit(1)
1 = Enabled
0 = Disabled

Note 1: This bit is only implemented on the PIC16F88. The bit will read '0' on the PIC16F87.

bit 5 **RCIE:** AUSART Receive Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 4 **TXIE:** AUSART Transmit Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 3 **SSPIE:** Synchronous Serial Port (SSP) Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 2 **CCP1IE:** CCP1 Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 1 **TMR2IE:** TMR2 to PR2 Match Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 0 **TMR1IE:** TMR1 Overflow Interrupt Enable bit
1 = Enabled
0 = Disabled

REGISTER 2-5: PIR1: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1 (ADDRESS 0Ch)

U-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0
—	ADIF(1)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6 **ADIF:** A/D Converter Interrupt Flag bit(1)
1 = The A/D conversion completed (must be cleared in software)
0 = The A/D conversion is not complete

Note 1: This bit is only implemented on the PIC16F88. The bit will read '0' on the PIC16F87.

bit 5 **RCIF:** AUSART Receive Interrupt Flag bit
1 = The AUSART receive buffer is full (cleared by reading RCREG)
0 = The AUSART receive buffer is not full

bit 4 **TXIF:** AUSART Transmit Interrupt Flag bit
1 = The AUSART transmit buffer is empty (cleared by writing to TXREG)
0 = The AUSART transmit buffer is full

bit 3 **SSPIF:** Synchronous Serial Port (SSP) Interrupt Flag bit
1 = The transmission/reception is complete (must be cleared in software)
0 = Waiting to transmit/receive

bit 2 **CCP1IF:** CCP1 Interrupt Flag bit
Capture mode:
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare mode:
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM mode:
Unused in this mode.

bit 1 **TMR2IF:** TMR2 to PR2 Interrupt Flag bit
1 = A TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 to PR2 match occurred

bit 0 **TMR1IF:** TMR1 Overflow Interrupt Flag bit
1 = The TMR1 register overflowed (must be cleared in software)
0 = The TMR1 register did not overflow

REGISTER 2-6: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2 (ADDRESS 8Dh)

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0
OSFIE	CMIE	—	EEIE	—	—	—	—
bit 7							bit 0

bit 7 **OSFIE:** Oscillator Fail Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 6 **CMIE:** Comparator Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **EEIE:** EEPROM Write Operation Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 3-0 **Unimplemented:** Read as '0'

REGISTER 2-7: PIR2: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 2 (ADDRESS 0Dh)

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0
OSFIF	CMIF	—	EEIF	—	—	—	—
bit 7							bit 0

bit 7 **OSFIF:** Oscillator Fail Interrupt Flag bit
1 = System oscillator failed. clock input has changed to INTRC (must be cleared in software)
0 = System clock operating

bit 6 **CMIF:** Comparator Interrupt Flag bit
1 = Comparator input has changed (must be cleared in software)
0 = Comparator input has not changed

bit 5 **Unimplemented:** Read as '0'

bit 4 **EEIF:** EEPROM Write Operation Interrupt Flag bit
1 = The write operation completed (must be cleared in software)
0 = The write operation is not complete or has not been started

bit 3-0 **Unimplemented:** Read as '0'

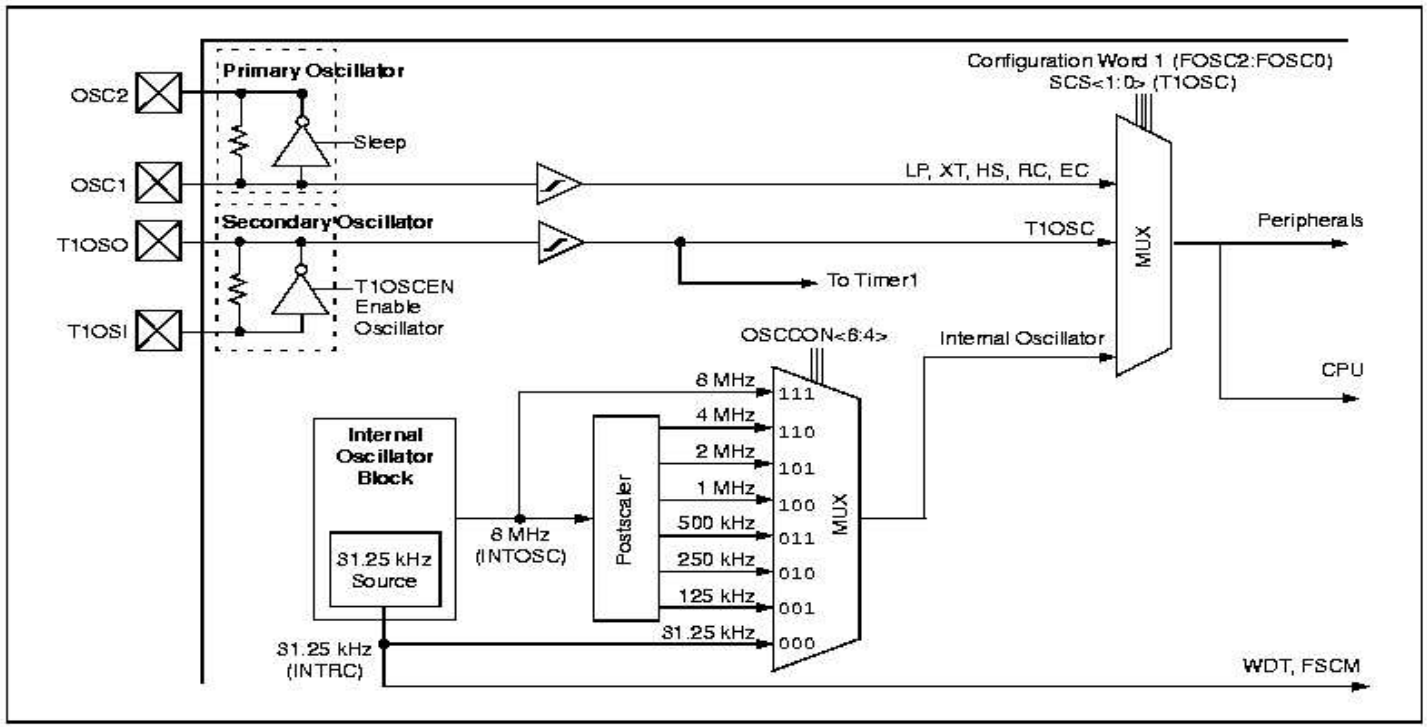
El oscilador

MODOS

1. LP — Low-Power Crystal
2. XT — Crystal/Resonator
3. HS — High-Speed Crystal/Resonator
4. RC — External Resistor/Capacitor with Fosc/4 output on RA6
5. RCIO — External Resistor/Capacitor with I/O on RA6
6. INTIO1 — Internal Oscillator with Fosc/4 output on RA6 and I/O on RA7
7. INTIO2 — Internal Oscillator with I/O on RA6 and RA7
8. ECIO — External Clock with I/O on RA6

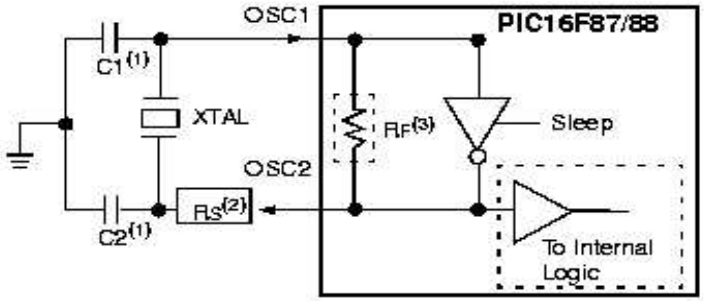
Osc Type	Crystal Freq	Typical Capacitor Values Tested:	
		C1	C2
LP	32 kHz	33 pF	33 pF
XT	200 kHz	56 pF	56 pF
	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

FIGURE 4-6: PIC16F87/88 CLOCK DIAGRAM



conexión del oscilador

FIGURE 4-1: CRYSTAL OPERATION (HS, XT, OR LP OSCILLATOR CONFIGURATION)



Note1: See Table 4-1 for typical values of C1 and C2.

2: A series resistor (RS) may be required for AT strip cut crystals.

3: RF varies with the crystal chosen (typically between 2 MΩ to 10 MΩ).

FIGURE 4-3: EXTERNAL CLOCK INPUT OPERATION (ECIO CONFIGURATION)

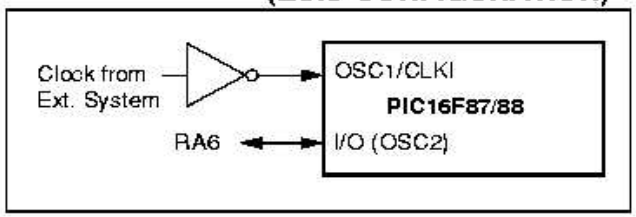


FIGURE 4-4: RC OSCILLATOR MODE

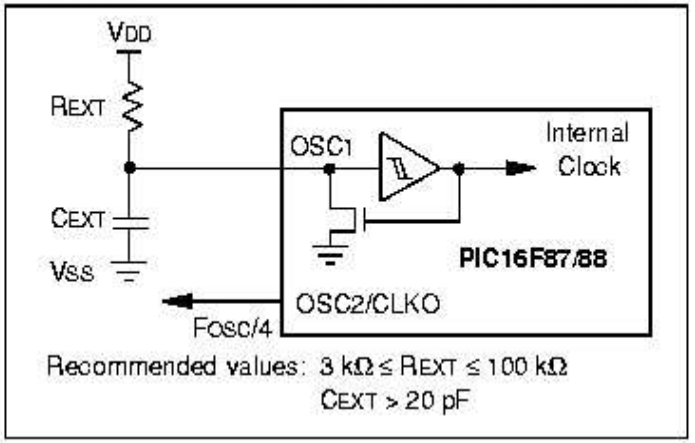
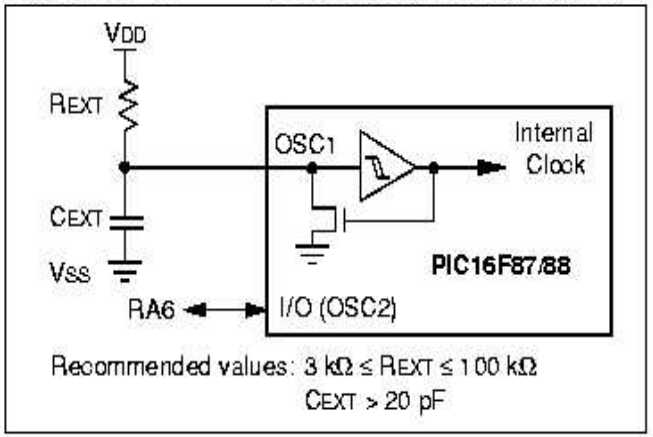


FIGURE 4-5: RCIO OSCILLATOR MODE



Registros de control del oscilador

REGISTER 4-1: OSCTUNE: OSCILLATOR TUNING REGISTER (ADDRESS 90h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** Frequency Tuning bits

011111 = Maximum frequency
011110 =
•
•
•
000001 =
000000 = Center frequency. Oscillator module is running at the calibrated frequency.
111111 =
•
•
•
100000 = Minimum frequency

- OSCTUNE -> ajuste del oscilador
  - Oscilador calibrado de fábrica
  - OSCTUNE permite ajustarlo en un ±12.5%
- OSCCON -> configuración del oscilador

REGISTER 4-2: OSCCON: OSCILLATOR CONTROL REGISTER (ADDRESS 8Fh)

U-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0
—	IRCF2	IRCF1	IRCF0	OSTS(1)	IOFS	SCS1	SCS0
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **IRCF<2:0>:** Internal RC Oscillator Frequency Select bits

000 = 31.25 kHz
001 = 125 kHz
010 = 250 kHz
011 = 500 kHz
100 = 1 MHz
101 = 2 MHz
110 = 4 MHz
111 = 8 MHz

bit 3 **OSTS:** Oscillator Start-up Time-out Status bit(1)

1 = Device is running from the primary system clock
0 = Device is running from T1OSC or INTRC as a secondary system clock

Note 1: Bit resets to '0' with Two-Speed Start-up mode and LP, XT or HS selected as the oscillator mode.

bit 2 **IOFS:** INTOSC Frequency Stable bit

1 = Frequency is stable
0 = Frequency is not stable

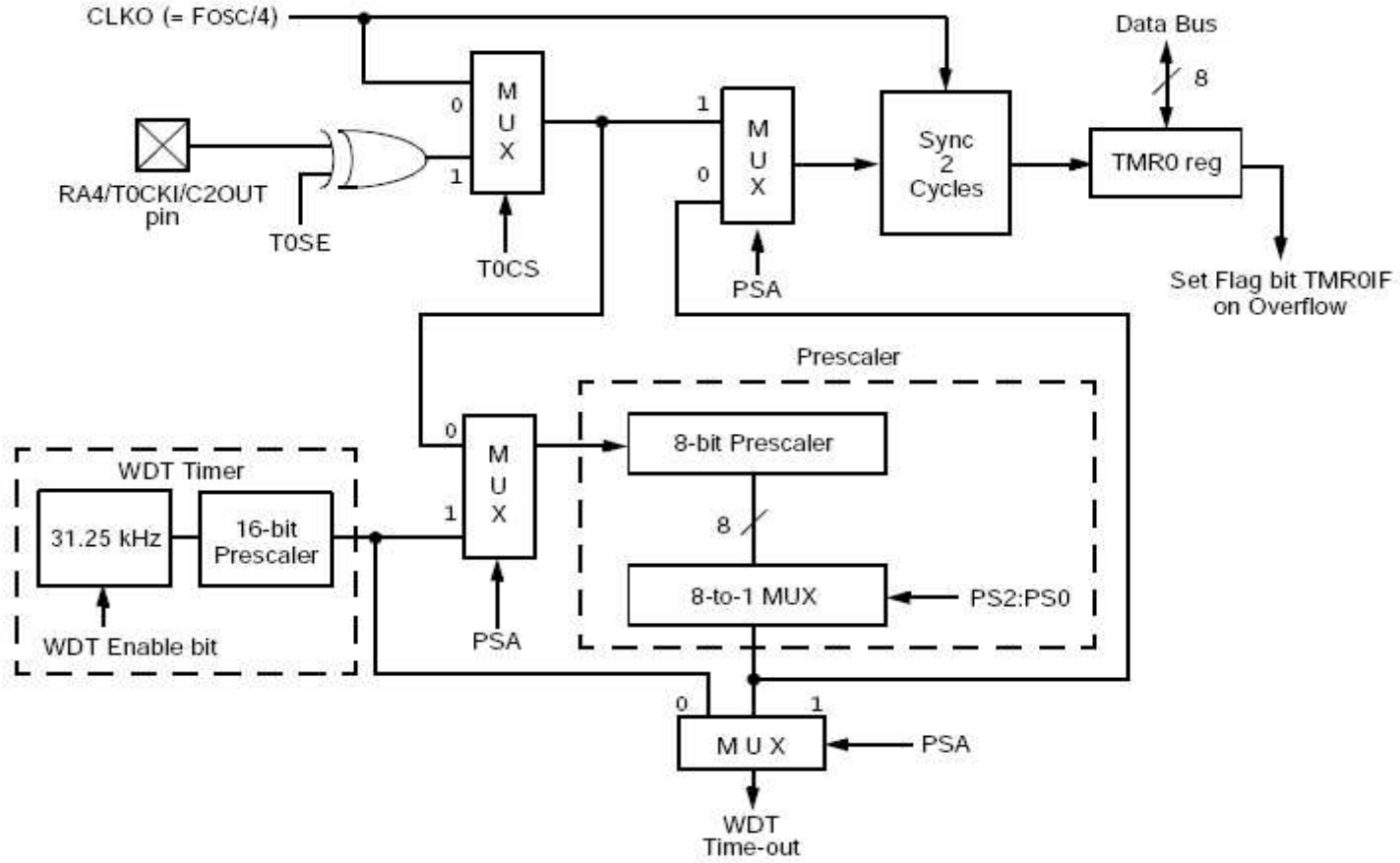
bit 1-0 **SCS<1:0>:** Oscillator Mode Select bits

00 = Oscillator mode defined by FOSC<2:0>
01 = T1OSC is used for system clock
10 = Internal RC is used for system clock
11 = Reserved

Temporizadores

- TMR0 -> igual que en PIC16F84 (8 bits)
- WDT -> igual que en PIC16F84 pero con un prescaler exclusivo de 16 bits (además del prescaler compartido de 8 bits)
- TMR1
  - Temporizador de 16 bits
  - Puede usarse como reloj secundario en modos de bajo consumo
  - Puede usarse como reloj de tiempo real (RTC)
  - Genera interrupción en desbordamiento
- TMR2
  - Temporizador de 8 bits
  - Prescaler y postscaler
  - Genera interrupción en desbordamiento

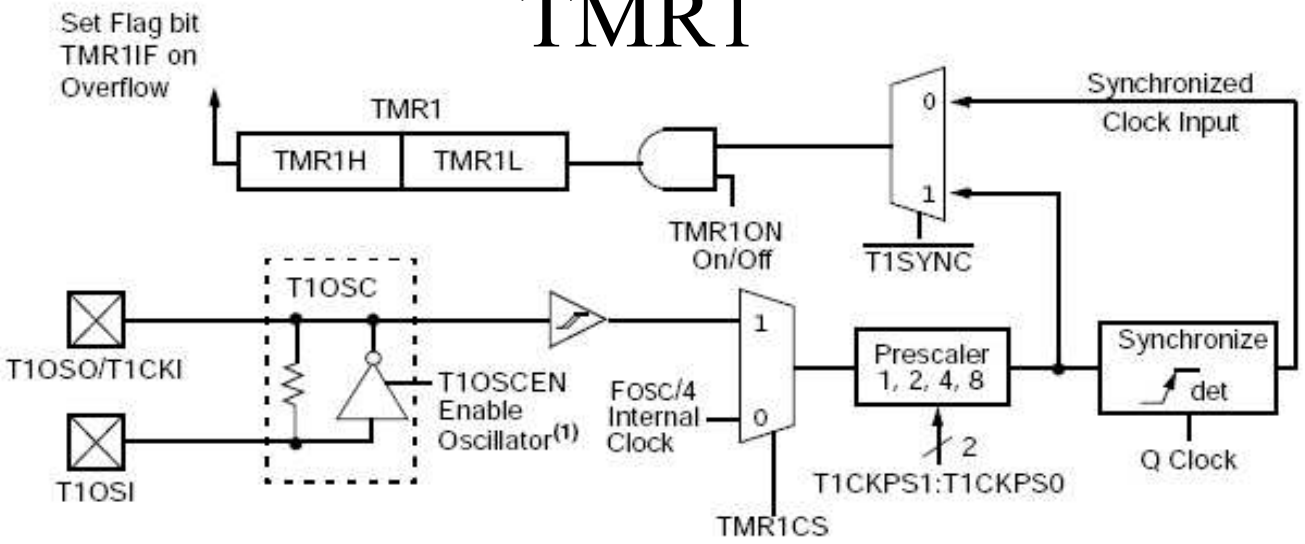
TMR0 y WDT



Note: T0CS, T0SE, PSA and PS2:PS0 bits are (OPTION_REG<5:0>).

- Iguales que en PIC16F84
- Prescaler de 16 bit en WDT -> permite
  - Usar prescaler 16 bit en WDT y prescaler 8 bit en TMR0 simultaneamente
  - Prescindir de prescaler en TMR0 y usar prescaler de 24 bits en WDT

TMR1



Note 1: When the T1OSCEN bit is cleared, the inverter is turned off. This eliminates power drain.

- Características:
  - Temporizador de 16 bits -> registros TMR1H:TMR1L, con prescaler 1:8
  - Interrupción en desbordamiento
    - Flag TMR1IF (registro PIR1)
    - Enmascarable con TMR1IE (registro PIE1)
  - Modos de funcionamiento
    - Temporizador (igual que TMR0, pero con 16 bits)
    - Contador -> funcionamiento síncrono/asíncrono

Registro de control del TMR1

REGISTER 7-1: T1CON: TIMER1 CONTROL REGISTER (ADDRESS 10h)

U-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6 **T1RUN**: Timer1 System Clock Status bit
1 = System clock is derived from Timer1 oscillator
0 = System clock is derived from another source

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3 **T1OSCEN:** Timer1 Oscillator Enable Control bit
1 = Oscillator is enabled
0 = Oscillator is shut off (the oscillator inverter is turned off to eliminate power drain)

bit 2 **$\overline{\text{T1SYNC}}$:** Timer1 External Clock Input Synchronization Control bit
TMR1CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
TMR1CS = 0:
This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

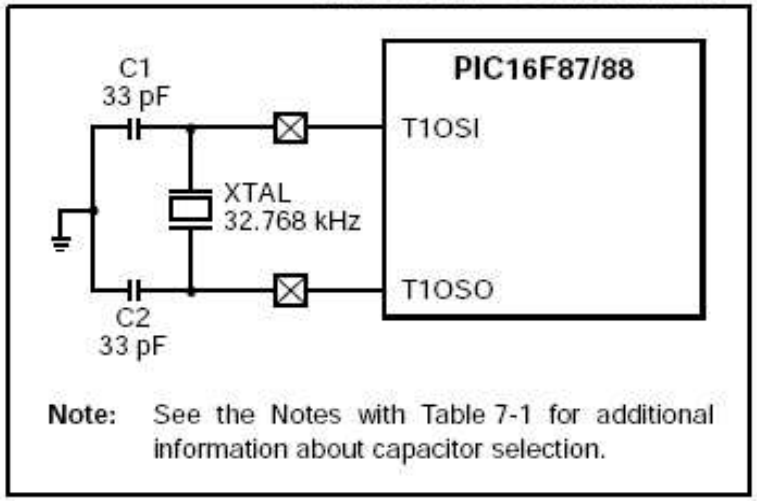
bit 1 **TMR1CS:** Timer1 Clock Source Select bit
1 = External clock from pin RB6/AN5(1)/PGC/T1OSO/T1CKI (on the rising edge)
0 = Internal clock (Fosc/4)

Note 1: Available on PIC16F88 devices only.

bit 0 **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

- Modos de funcionamiento
  - Modo temporizador
    - Se selecciona con TMR1CS = 0
    - En este modo el temporizador funciona con $F_{OSC}/4$
  - Modo contador
    - Se selecciona con TMR1CS = 1
    - Puede funcionar con
      - Reloj externo (pin T1CKI) -> si configuramos T1OSCEN = 1
      - Reloj interno (con cristal LP) -> si configuramos T1OSCEN = 0
      - En ambos casos puede configurarse en modo síncrono o asíncrono
    - Modo contador síncrono (T1SYNC = 0)
      - Sincroniza el reloj con el reloj interno
      - En modo sleep se para el reloj
    - Modo contador asíncrono (T1SYNC = 1)
      - No sincroniza el reloj
      - TMR1 sigue contando durante SLEEP => puede despertar al micro

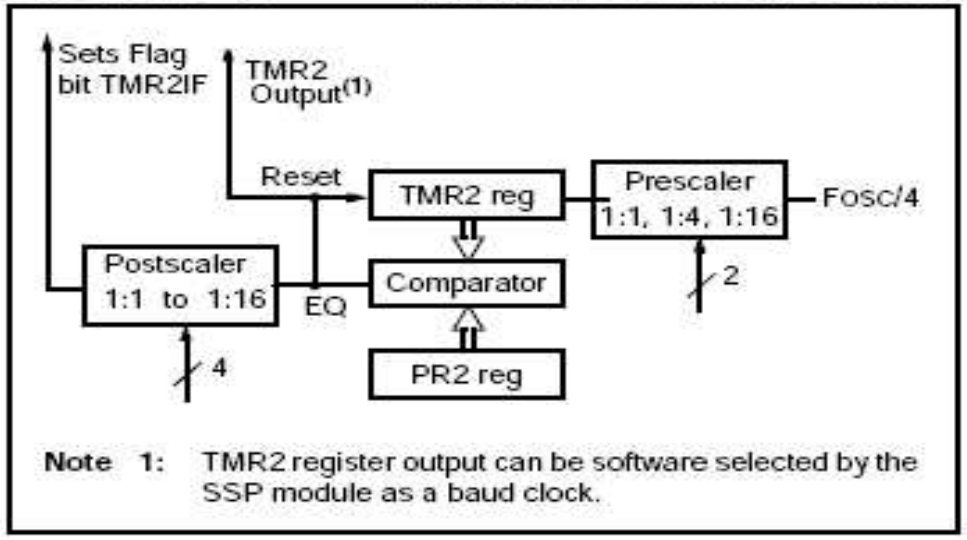
FIGURE 7-3: EXTERNAL COMPONENTS FOR THE TIMER1 LP OSCILLATOR



Note: See the Notes with Table 7-1 for additional information about capacitor selection.

TMR2

FIGURE 8-1: TIMER2 BLOCK DIAGRAM



- Características:
  - Temporizador de 8 bits -> registro TMR2 (cuenta) PR2 (limite)
  - Prescaler 1:8 y postscaler 1:16
  - Interrupción cuando TMR coincide con PR2
    - Flag TMR2IF (registro PIR1)
    - Enmascarable con TMR2IE (registro PIE1)
  - Se puede usar como base de tiempos para el módulo PWM / CCP

REGISTER 8-1: T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6-3 **TOUTPS<3:0>:** Timer2 Output Postscale Select bits

0000 = 1:1 Postscale
0001 = 1:2 Postscale
0010 = 1:3 Postscale
•
•
•
1111 = 1:16 Postscale

bit 2 **TMR2ON:** Timer2 On bit

1 = Timer2 is on
0 = Timer2 is off

bit 1-0 **T2CKPS<1:0>:** Timer2 Clock Prescale Select bits

00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16

TABLE 8-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF(1)	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
8Ch	PIE1	—	ADIE(1)	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
11h	TMR2	Timer2 Module Register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
92h	PR2	Timer2 Period Register								1111 1111	1111 1111

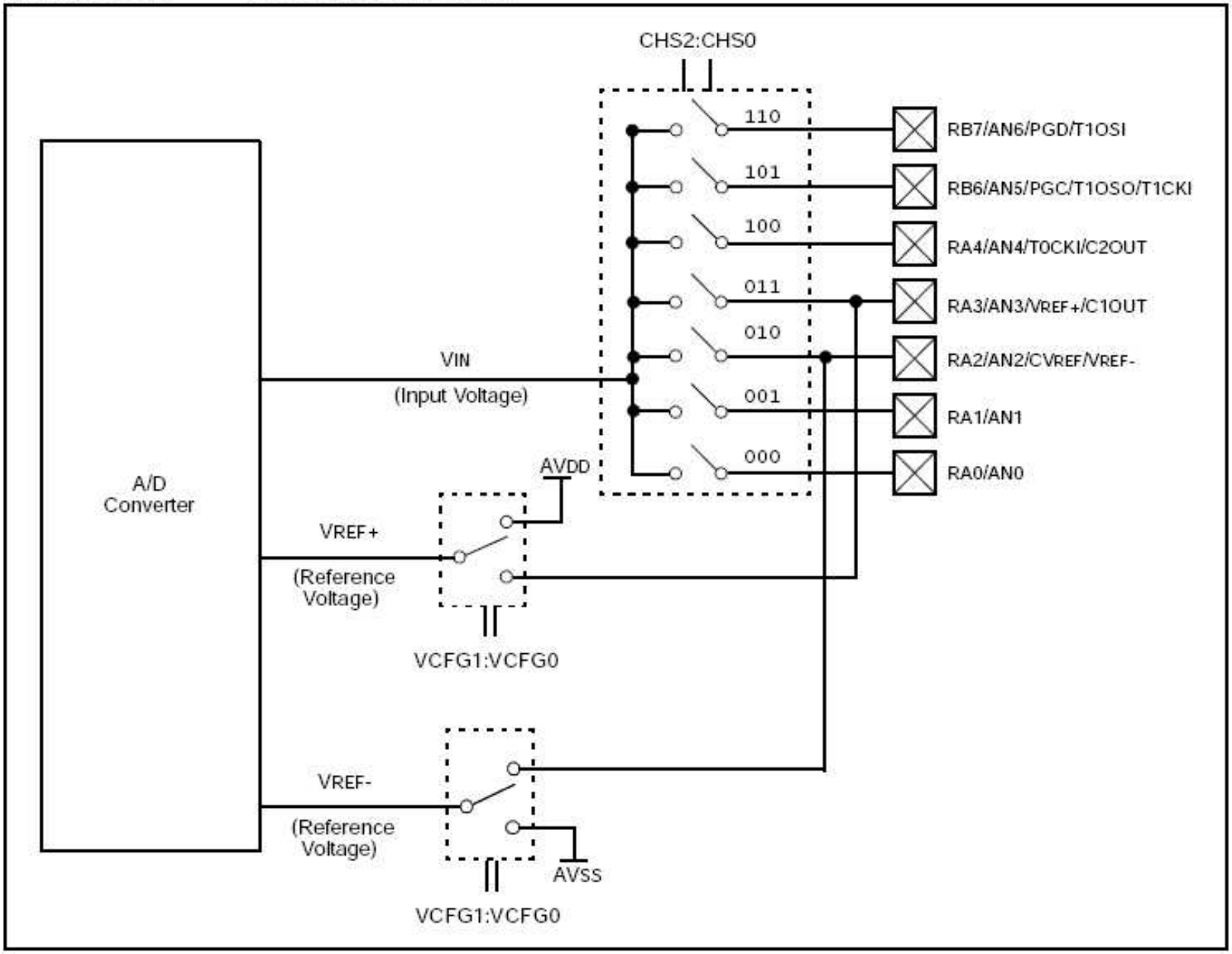
Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer2 module.

Note 1: This bit is only implemented on the PIC16F88. The bit will read '0' on the PIC16F87.

Convertidor A/D

- Características
  - 7 entradas analógicas (7 canales)
  - A/D de 10 bits
  - Referencias positivas (V_{REF+}) y negativas (V_{REF-}) seleccionables
  - Posibilidad de trabajar en modo sleep usando el oscilador RC interno.
- Registros de control
  - ADRESH -> parte alta del resultado
  - ADRESL -> parte baja del resultado
  - ADCON0 / ADCON1 -> registros de control
  - ANSEL -> registro de selección de entradas analógicas

FIGURE 12-1: A/D BLOCK DIAGRAM



Operación del ADC

- Configurar el módulo A/D (secuencia)
  - Configurar los pines I/O como analógicos/digitales (ANSEL)
  - Configurar la tensión de referencia (ADCON1)
  - Seleccionar el canal de entrada A/D (ADCON0)
  - Seleccionar la fuente de reloj del ADC (ADCON0)
  - Activar el módulo A/D (ADCON0)
- Configurar la interrupción A/D (opcional)
  - ADIF=0, ADIE=1, PEIE=1, GIE=1
- Adquisición de un dato
  - Fijar la señal GO/$\overline{\text{DONE}}$ = 1 (ADCON0)
  - Esperar a la interrupción, o a que GO/$\overline{\text{DONE}}$ se ponga a cero
  - Leer el dato de ADRESH:ADRESL
  - Borrar ADIF si se está usando la interrupción

Registros de control

REGISTER 12-1: ANSEL: ANALOG SELECT REGISTER (ADDRESS 9Bh) PIC16F88 DEVICES ONLY

U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0
bit 7							bit 0

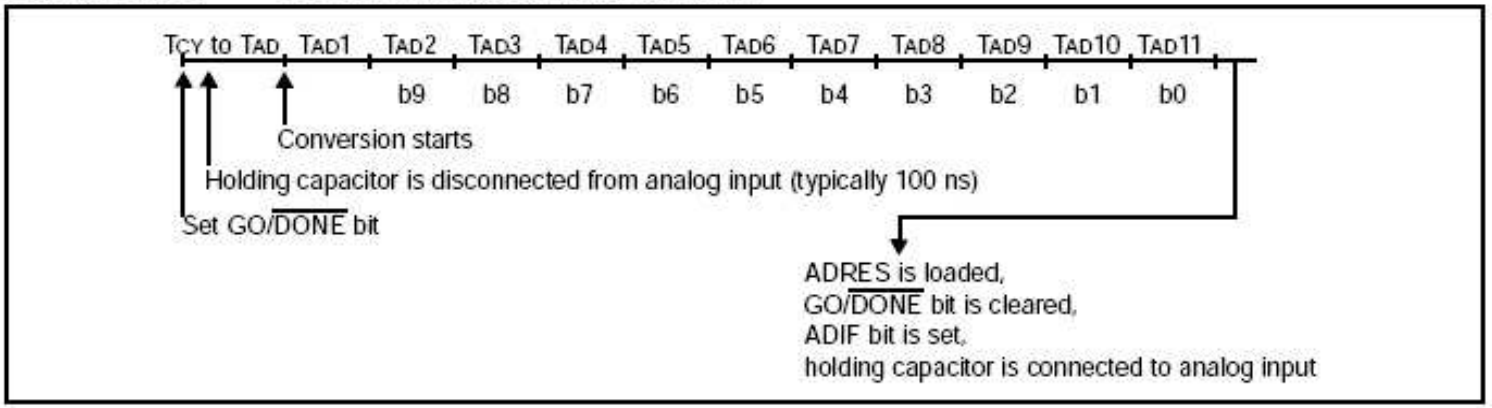
bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ANS<6:0>:** Analog Input Select bits
Bits select input function on corresponding AN<6:0> pins.
1 = Analog I/O(1,2)
0 = Digital I/O

Note 1: Setting a pin to an analog input disables the digital input buffer. The corresponding TRIS bit should be set to input mode when using pins as analog inputs. Only AN2 is an analog I/O, all other ANx pins are analog inputs.

2: See the block diagrams for the analog I/O pins to see how ANSEL interacts with the CHS bits of the ADCON0 register.

FIGURE 12-3: A/D CONVERSION TAD CYCLES



REGISTER 12-2: ADCON0: A/D CONTROL REGISTER (ADDRESS 1Fh) PIC16F88 DEVICES ONLY

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON
bit 7							bit 0

bit 7-6 **ADCS<1:0>:** A/D Conversion Clock Select bits

If ADCS2 = 0:
00 = Fosc/2
01 = Fosc/8
10 = Fosc/32
11 = FRC (clock derived from the internal A/D module RC oscillator)

If ADCS2 = 1:
00 = Fosc/4
01 = Fosc/16
10 = Fosc/64
11 = FRC (clock derived from the internal A/D module RC oscillator)

bit 5-3 **CHS<2:0>:** Analog Channel Select bits

000 = Channel 0 (RA0/AN0)
001 = Channel 1 (RA1/AN1)
010 = Channel 2 (RA2/AN2)
011 = Channel 3 (RA3/AN3)
100 = Channel 4 (RA4/AN4)
101 = Channel 5 (RB6/AN5)
110 = Channel 6 (RB7/AN6)

bit 2 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit

If ADON = 1:
1 = A/D conversion in progress (setting this bit starts the A/D conversion)
0 = A/D conversion not in progress (this bit is automatically cleared by hardware when the A/D conversion is complete)

bit 1 **Unimplemented:** Read as '0'

bit 0 **ADON:** A/D On bit

1 = A/D converter module is operating
0 = A/D converter module is shut off and consumes no operating current

REGISTER 12-3: ADCON1: A/D CONTROL REGISTER 1 (ADDRESS 9Fh) PIC16F88 DEVICES ONLY

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
ADFM	ADCS2	VCFG1	VCFG0	—	—	—	—
bit 7							bit 0

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified. Six Most Significant bits of ADRESH are read as '0'.
0 = Left justified. Six Least Significant bits of ADRESL are read as '0'.

bit 6 **ADCS2:** A/D Clock Divide by 2 Select bit
1 = A/D clock source is divided by 2 when system clock is used
0 = Disabled

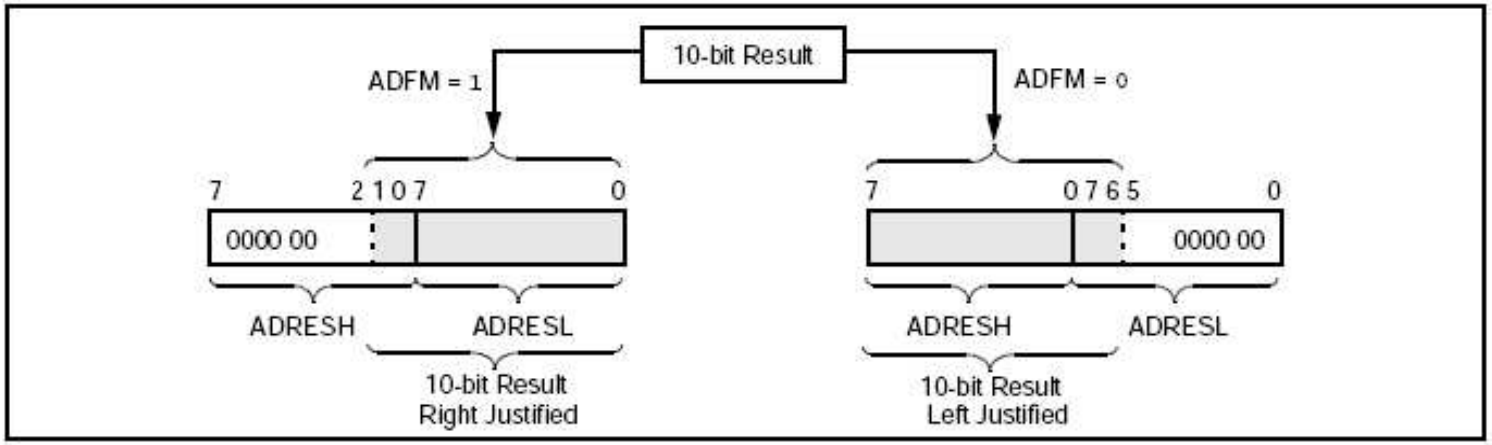
bit 5-4 **VCFG<1:0>:** A/D Voltage Reference Configuration bits

Logic State	VREF+	VREF-
00	AVDD	AVSS
01	AVDD	VREF-
10	VREF+	AVSS
11	VREF+	VREF-

Note: The ANSEL bits for AN3 and AN2 inputs must be configured as analog inputs for the VREF+ and VREF- external pins to be used.

bit 3-0 **Unimplemented:** Read as '0'

FIGURE 12-4: A/D RESULT JUSTIFICATION



- Tiempos en la conversión A/D
  - Tiempo de Adquisición
    - Tiempo desde que se selecciona el canal hasta que se puede lanzar la conversión (Activar GO/DONE)
    - Tiempo mínimo: $T_{ACQ} = 19{,}72\mu s$
  - Tiempo de conversión
    - Tiempo desde que se inicia la conversión hasta que termina
    - $T_C = 9\ T_{AD}$
    - T_{AD} es el periodo del reloj de conversión, seleccionable

TABLE 12-1: TAD vs. MAXIMUM DEVICE OPERATING FREQUENCIES – STANDARD DEVICES (C)

AD Clock Source (TAD)			Maximum Device Frequency
Operation	ADCS<2>	ADCS<1:0>	Max.
2 Tosc	0	00	1.25 MHz
4 Tosc	1	00	2.5 MHz
8 Tosc	0	01	5 MHz
16 Tosc	1	01	10 MHz
32 Tosc	0	10	20 MHz
64 Tosc	1	10	20 MHz
RC(1,2,3)	x	11	(Note 1)

Note 1: The RC source has a typical TAD time of 4 µs, but can vary between 2-6 µs.

2: When the device frequencies are greater than 1 MHz, the RC A/D conversion clock source is only recommended for Sleep operation.

3: For extended voltage devices (LF), please refer to **Section 18.0 "Electrical Characteristics"**.